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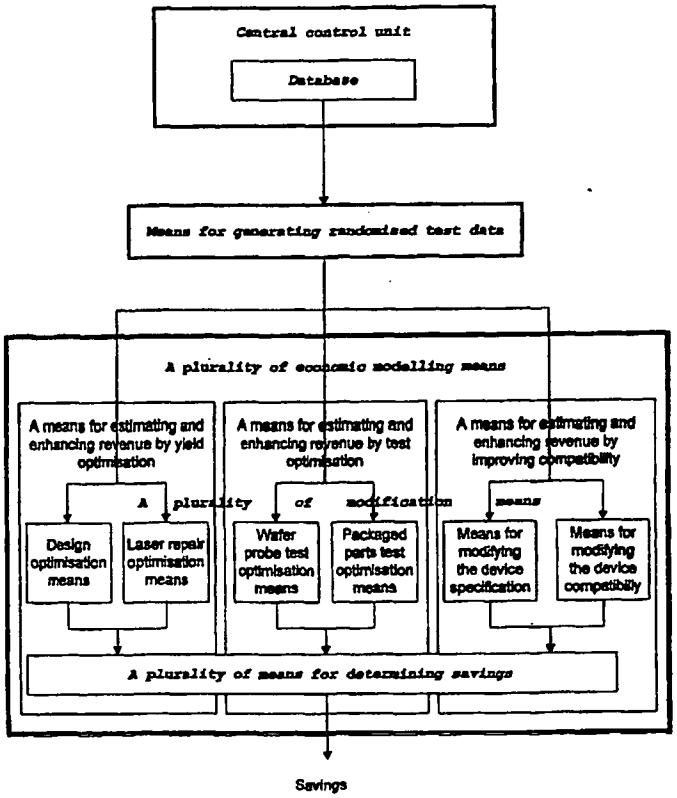
(54) Title: A SYSTEM FOR MODELLING MEMORY BUSINESS PARAMETERS

(57) Abstract

A system for modelling memory business parameters provides the key competitive advantages for companies in the memory industry by optimising each step in the product flow to achieve the maximum number of products shipped at the lowest cost and with the optimum level of application compatibility. This system creates a model using various business parameters, such as memory design, processing costs, production capacity and characteristics, technology limits, user demand, and end application compatibility. Using this model, the system then estimates the profitability of a memory industry plant in terms of finished good devices as a function of the cost of sales, based on possible variations of business parameters and predicts the savings that may be obtained if business parameters are optimised.



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A System for Modelling Memory Business Parameters

Technical field

The present invention relates to a system for analysis of statistical data and enhancement of profitability in the memory manufacturing industry, and, more particularly, to a system for profiling and modelling the economical performance of the memory business and a method for estimating revenue and enhancing the same by increasing production yield and/or achieving a high compatibility level for the memory devices produced and/or optimising or shortening test processes.

The present invention is applicable in particular, though not exclusively, to software-implemented systems for analysis, modification and optimisation of various parameters at different stages of the memory manufacturing process, including specification and design parameters, fabrication process parameters, wafer and die level testing procedures parameters, laser repair process and packaged chip testing parameters. It can also be used to improve compatibility and to view the actual results of various improvement operations in order to estimate and enhance their effectiveness and consequently the profitability of a memory business.

Background art

In the semiconductor memory industry, memory devices are fabricated on silicon wafers, typically 400 die per wafer. The design of the wafer greatly influences the yield. A 1% yield improvement achieved by modifying design parameters, such as layout topology, may be worth over 10 M$ per year. Even a modest yield improvement can be extremely significant. The wafer products obtained are tested after fabrication using automated testing equipment. For a particular memory architecture, some test methods have higher defect coverage than others. After test, the wafer is sliced into dies; the good dies are packaged, burnt in and re-tested. Modelling schemes, e.g. optimisation models, are known for some steps of the product flow, however, it is difficult to achieve simultaneous optimisation of different performance criteria and to estimate their cost effectiveness. Companies generally use heuristically determined methods to support the simultaneous achievement of high yield and economic performance.

Another important problem is achieving high end user compatibility. The specification used by a memory device customer does not match the datasheet issued by the memory manufacturer. End users have differing specification requirements. For

instance, a businessman involved in a fabrication process that includes designing a memory device, a company buying memory products for making modules, and a customer involved in testing memory products all have different requirements which do not match each other. Maximising compatibility for each different end-use is a major problem for the manufacturer. Poor compatibility jeopardises sales, increases customers' returns and results in a lower market value for the products.

Different attempts have been made to solve the above problems. Known are a computer-aided design system and method (see US 4922432) for designing an application specific integrated circuit which provides the user, upon defining the application specification, with the detailed information needed for directly producing the defined integrated circuit. The known system uses artificial intelligence and expert systems technology, however, the required solution is optimised from the point of view of the end specific application only, without taking into account the optimisation cost and possible savings obtainable through production of a customised product.

A system, method and software product for optimising the multiple performance criteria of integrated circuits are described in US 5663891. The use of the known computer-aided design apparatus provides a simultaneous optimisation of design and cost parameters to enhance production yield at minimum cost. The optimisation is achieved by converting a structural description of an integrated circuit into a constraint graph and modifying the graph to include cost functions for selected performance criteria. To create a model, the law of probability is used and several assumptions are made using average meanings. However, the known system is not adapted for assuring high compatibility of a particular memory device in a different user's application. Another disadvantage is that the actual test data and the number and distribution of defects are not taken into consideration when modelling the semiconductor device.

One more approach to the problem of memory device modelling is used in a means for optimising a semiconductor device fabrication flow on different levels by simulating the process and feeding the result of the simulation to a process flow preparation section (see US 5694325). The known system automatically provides the manufacturer with information for optimising production process parameters; however, the simulation results reflect the average, not the actual distribution of defects. Besides, the resulting revenues and possible savings are not taken into account.

By using the actual yield data and defect information from previously produced devices according to US 3751647, yield predictions may be made. The yield model is generated utilising the number of defects for each chip, rather than average defect density, and also includes some probability evaluations. However, the known method does not provide for using the information obtained to calculate any possible optimisation of costs and resulting savings to be achieved by modifying the process parameters in device yield modelling.

Thus, one of the key limitations of the known approaches is that memory manufacturing optimisation problems and compatibility problems are solved separately and apart from economic performance modelling. Where the process conditions are simulated, feedback of the simulation results and the process conditions is conducted according to a judgement of technical experts, consequently it is often impossible to perform appropriate feedbacks. Moreover, no means are offered for calculating optimisation costs and actual savings to allow a non-preconceived choice to be made between one or more possible process improvement steps. Another drawback is that the known systems are too complex and difficult to be used by an ordinary skilled operator or a businessman involved in a memory manufacturing industry.

Accordingly, it is desirable to provide a system for improving any one of a plurality of economic performance criteria, including yield, test and compatibility criteria, to enable a businessman in a memory industry, such as a manufacturing or a testing plant, not only to improve production profitability, but to estimate easily the savings and revenues resulting from optimisation.

Disclosure of Invention

The substance of the present invention is a system for modelling the business parameters of the memory industry using back end test data and a structural description of the memory device stored in a database, the system comprising an economic modelling means for profiling and modelling the economic performance of the business. The system preferably includes also a randomisation means for generating randomised back end test data to use when creating a business model. The proposed economic modelling means comprises at least one means for estimating and enhancing the profitability of a memory industry plant, selected from: a means for estimating and enhancing revenue by yield optimisation. a means for estimating and enhancing profits by test optimisation and a

means for estimating and enhancing revenue by improving compatibility (see Fig.1). Though the said combination has proven to be particularly effective in enhancing the profits of memory business, the above means can also be used separately or in different combinations to improve certain economic parameters mentioned above.

The main advantage of the proposed system is that it improves engineering criteria including yield, test and compatibility criteria, as well as creating an economic model, using back end test data and a structural description of a memory device stored in a database, which allows the actual profits achieved by the improvements to be calculated. Despite the common opinion, that using back end test data does not allow the production process to be estimated adequately, the use of highly randomised statistical methods to alter the actual back end data, in order to produce a set of data with characteristics expected at a future evolutionary step in process development, enables a precise estimation of product flow parameters to be made.

In the system for modelling the parameters of a memory device business in accordance with the present invention, the means for estimating and enhancing the revenue by optimising the yield in terms of the number of finished working devices as a function of the cost of goods may be represented by at least one means selected from: a means for estimating and enhancing revenue at memory design optimisation and a means for estimating and enhancing revenue at laser repair process optimisation. Further, the means for estimating and enhancing revenue by test optimisation may comprise at least one means selected from: a means for estimating and enhancing revenue at wafer probe test optimisation and a means for estimating and enhancing revenue at package test optimisation.

The means for estimating and enhancing revenue by improving compatibility includes at least one means selected from: a means for estimating and enhancing revenue at modifying the device specification, a means for estimating and enhancing revenue at modifying the device compatibility, and a means for estimating and enhancing revenue at incoming inspection by the end user or buyer.

According to one embodiment of the present invention, the system for modelling a memory device business is adapted for estimating and enhancing the profitability of a plant wherein memories are designed, fabricated, tested and shipped in the form of chips or wafer products. The system comprises the following combination of economic

modelling means: a means for estimating and enhancing the revenue by modifying the device specification, a means for estimating and enhancing revenue at memory design optimisation, a means for estimating and enhancing profits at wafer probe test sequence optimisation, a means for estimating and enhancing the revenue at laser repair process optimisation, a means for estimating and enhancing profits at package test optimisation, a means for estimating and enhancing revenue at modifying compatibility (see Fig.2).

According to another embodiment of the present invention, the system for modelling a memory device business is adapted for estimating and enhancing the profitability of a memory module manufacturing process and comprises: a means for estimating and enhancing revenue by modifying the device specification parameters, a means for estimating and enhancing revenue at incoming inspection, a means for estimating and enhancing profits at wafer probe test sequence optimisation, a means for estimating and enhancing revenue at laser repair process optimisation, a means for estimating and enhancing profits at package test optimisation, and a means for estimating and enhancing revenue by modifying the device compatibility.

According to another embodiment of the present invention, the system for modelling a memory device business is adapted for estimating and enhancing the profitability of a memory device testing process and includes: a means for estimating and enhancing revenue at incoming inspection, a means for estimating and enhancing profits at wafer probe test optimisation, a means for estimating and enhancing revenue at laser repair optimisation, a means for estimating and enhancing profits at package test optimisation, a means for estimating and enhancing revenue at modifying the device compatibility (see Fig.3).

According to another embodiment of the present invention, the system for modelling a memory device business is adapted for estimating and enhancing the profitability of a memory plant where wafers are fabricated and tested for customers, and includes: a means for estimating and enhancing revenue by modifying the device specification parameters, a means for estimating and enhancing revenue at incoming inspection, and a means for estimating and enhancing profits at wafer probe test sequence optimisation.

Another aspect of the present invention is a method for estimating and enhancing the profitability of a memory industry plant by modelling the business using back end test

data and a structural description of a memory device stored in a database. The method includes a step of estimating and enhancing revenue by yield optimisation, a step of estimating and enhancing profits by test optimisation and a step of estimating and enhancing revenue by modifying compatibility, the steps may be performed while using the above system in accordance with the present invention. Statistically randomised back end test data shall preferably be used for creating a business model. Another aspect of the present invention is a computer implemented method for profiling and modelling the economic performance of a memory device business using back end test data and a structural description of a memory device stored in a database.

Another aspect of the present invention is a computer aided design device that uses the proposed system or method according to the present invention. Yet another aspect of the present invention is a computer readable memory operable in a computer aided design device, the computer readable memory comprising a computer program for performing a computer implemented method according to the present invention. A computer program for implementing or emulating or simulating the hardware functions of a system, device or method, when stored in electrically readable media has also been proposed.

Brief Description of Drawings

For a better understanding of the present invention and to show how the same may be carried into effect, reference will now be made, by way of example, without loss of generality, to the accompanying drawings in which:

Fig. 1 shows the block scheme of the business modelling system in accordance with the present invention.

Fig. 2 shows the block scheme of the business modelling system in accordance with the first embodiment of the present invention.

Fig. 3 shows the block scheme of the business modelling system in accordance with the third embodiment of the present invention.

Fig. 4 shows an example flow chart of the operation of the means for estimating and enhancing profits by modifying the device specification.

Fig. 5 shows an example flow chart of the operation of the means for estimating and enhancing revenue at design optimisation.

Fig. 5a shows the results of design optimisation by tile number for a lot of 10 BNCHMRK chips and a lot of 15 BNCHMRK chips.

Fig. 5b shows the results of optimisation by aspect ratio for a lot of 10 BNCHMRK chips and a lot of 15 BNCHMRK chips.

Fig. 5c shows the results of optimisation by spare number for a lot of 10 BNCHMRK chips and a lot of 15 BNCHMRK chips.

Fig. 5d illustrates the results of optimisation by number of global spares for a lot of 10 BNCHMRK chips and a lot of 15 BNCHMRK chips.

Fig. 5e illustrates the results of optimisation by architecture for a lot of 10 BNCHMRK chips and a lot of 15 BNCHMRK chips.

Fig. 6 shows an example flow chart of the operation of the means for estimating and enhancing profits at wafer probe test optimisation.

Fig. 7 shows an example time graph for the optimised wafer probe test sequence.

Fig. 8 shows an example flow chart of the operation of the means for estimating and enhancing revenue at laser repair optimisation.

Fig. 8a illustrates the operation of the means for achieving laser optimisation by tuning redundancy allocation procedures for a lot of 10 BNCHMRK chips and a lot of 15 BNCHMRK chips.

Fig. 9 shows an example flow chart of the operation of the means for estimating and enhancing profits at package test optimisation.

Fig. 10 shows an example flow chart of the operation of the means for estimating and enhancing revenue by modifying the device compatibility.

Detailed Disclosure of Invention

Referring to Fig.1, an illustration of a system for modelling memory business parameters is shown in accordance with one embodiment of the present invention. The system may be implemented in hardware coupled with a central control unit which may be a conventional computer having a conventional memory, processor and operating system, or in software operable in the conventional computer. Various executable software modules are provided that configure and control the operation of the computer in accordance with the present invention. The system comprises a plurality of economic modelling means operable in conjunction with a database and a means for randomisation of back end test data coupled to the computer through conventional interfaces.

The layout database stores a symbolic structural description of a memory device. The structural description is comprised of layout objects, or cells, each addressable cell

having (X,Y) coordinates. The structural description also includes the following information about the memory device: a) chip type, i.e. memory device architecture, including the number of memory bits per tile; b) redundancy architecture, i.e., quantity, distribution and length of spare rows and columns available within the memory. On the basis of this information, the area of the memory is divided into separately treatable areas called tiles. Different types of spare resources are possible. In the structural description used according to the present invention, shared spare resources and global spare resources, i.e. spare rows or columns available for all tiles on the die, are used as well as spare elements available for one tile only. Each resource element is assigned a corresponding cost. The database also stores full defect information about representative batches of devices (called lots) produced by different manufacturers, including the defect map and test sequence used to test the device. The layout database may provide the structural description in a specially designed for this purpose format, or any customer defined symbolic format.

The means for test data randomisation generates a coverage map which shows the coverage of different types of defects found by different test sequences. This map is obtained by using: a) "defect-type" distribution parameters, and b) correlation parameters between the coverage of different types of defects achieved by using different test sequences.

Referring to Fig. 2, the operation scheme of the system for modelling a memory device business in accordance with the first embodiment of the present invention will now be explained in detail. Memory architecture information, standard test results and/or datasheets, and results obtained after testing memory products on application pods, including actual timings and functional data, stored in database 10, are entered either directly, or through the randomisation means, into a means 12 for modifying the device specification parameters, proposed in the present invention, which produces the worst case datasheet with the timings, voltage and refresh rate values which cause most memory devices failures. The means 14 calculates the savings achieved by avoiding possible failures and producing a customised memory device. The resulting information may be fed back to the design optimisation means 16. As the design of the wafer greatly influences the yield, design optimisation is carried out by design optimisation means 16 to obtain the maximum number of working dies per wafer. Any suitable design optimisation means

may be used (see, e.g. US 5663891). Especially recommendable is the design optimisation means proposed in the present invention, which provides optimisation by multiple memory architecture parameters using statistically randomised back end test data. The optimisation may be carried out by tile number per die, by distribution of local and global spares, by quantity of each type of spare element, by location of spares, by spare element size, etc. The results are used in a means 18 for determining savings at memory design optimisation. For early identification of the process problems and structures on the chip which are most likely to fail, the fabrication process parameters together with the information about optimised design may be analyzed at the process stage by the fabrication process optimisation means (see e.g. US 4901242, US 5694325). The results may be used for determining savings at fabrication process optimisation. The information relating to defect monitoring, including defect map and test coverage, is fed to a wafer test optimisation means 24. The wafer test optimisation means described, e.g. in UK 9716812.4, may be used for this purpose. The profits achieved by using an optimised and/or reduced wafer probe test sequence are calculated by a means 26 for determining savings at test optimisation. After performing the testing procedure, the wafer is sliced into dies, the good dies are packaged, burnt in and retested. The data obtained from the design optimisation means 16 and data concerning different redundancy allocation procedures are used by a laser repair optimisation means 28. To chart the yield differences from different redundancy allocation procedures performed by the laser optimisation means 28 and calculate the savings obtained, a means 30 for determining savings at laser optimisation is used. The optimal test sequence is computed by a package test optimisation means 32. The savings produced by using the package test optimisation means 32 are calculated by a means 34 for determining savings at package test sequence optimisation. The results received from the means 12 for modifying the device specification are used by a means 36 for modifying the device compatibility which analyses the results of measuring data strobes generated by different motherboards to issue a compatibility list. A means 38 for determining revenue gained by maximising compatibility is used to calculate possible profits obtainable by producing highly compatible memory products.

The means for estimating and enhancing revenues by modifying the device specification is adapted for providing high end user application compatibility and thus increasing business profits. An example flow chart is shown in Fig. 4.

Firstly, the means for modifying the device specification takes the production information about a particular memory device, issued by the manufacturer, which may include product type and other characteristics, e.g. timing, voltage, and refresh rate values, along with actual test results received from a particular test application pod and/or standard automated testing equipment (ATE).

Any suitable application pods may be used, including emulators or engineering testers specially developed for this purpose, some low cost testers or, alternatively, the means for measuring data strobe, described in UK 9714130. The application pods are preconfigured with the full parametric, timing and functional characteristics of a wide range of motherboards and OEM acceptance tests to verify device and process compatibility. The results may be plotted in the form of a widely used Schmoo plot (see Van de Goor, A.J. "Testing Semiconductor Memories – Theory and Practice" J. Wiley & Sons, UK, 1991).

To issue the worst case memory device datasheet, the worst-case requirement for each application is configured on application pods and the sample batch of devices is screened on these pods. The defect information may be collected for each worst case requirement application by interfacing to any ATE with an error capture memory. The production information, information about defects, including the number of defects, the defect map and the sequence of tests needed to identify the defects, is compared then with the test results. A correlation diagram may be plotted to match production results (lot B) with the results obtained on the application pod (lot A). The correlation function is defined by two parameters, T1 (1,....i) and T2 (1,....i), where T1(i) is the number of defects found by test i from test sequence A, as a percentage of the number of defects found by any one test from test sequence B; and T2(i) – the number of defects found by test i from test sequence A, but not found by test sequence B, as a percentage of the number of defects found by test sequence B. The correlation function is defined as map (X,Y) = k, where k is the number of times a defect occurs at address (X,Y) in lot A. The correlation diagrams obtained may be also used in the data randomisation means.

The means for modifying the device specification compares the production information with the test results to issue a worst case memory device datasheet, and analyses the timings, voltage, and refresh rates obtained from tests on the application pods to determine which particular parameter values cause device failures. The results can be

fed to the memory device design stage. Thus, a detailed application report is issued specifying the variance including a worst case DRAM datasheet and the optimal application fields for each market segment.

The higher the product compatibility achieved thanks to modified specification, the higher the market price which may be set for the given chip or wafer product. For example, the price may be higher for items having an extended refresh period and/or fast access. However, in this case the increased test time should be taken into account. Revenues achieved by producing a customised product at a higher price may be calculated by the means for determining savings as follows:

$$S = N_{product}\,[(D_{2cost} - D_{1cost}) - (t_2 - t_1)\cdot T_{cost}],$$

where D_{1cost} ($) is the market price for an original chip or wafer product.
D_{2cost}($) is the market price for a customised chip or wafer product,
$N_{product}$ is the number of chips sold for the increased price.
T_{cost} is the test time cost in cents per device and per second
t_1 is the original test time, t_2 is the increased test time.

The means for estimating and enhancing revenues at design optimisation is adapted for obtaining the maximum number of working dies per wafer after laser repair and thus increasing business profits. Each aspect of the memory architecture is optimised based on the design constraints, area costs and defect probabilities for that structure (obtained from back end test results). In particular, redundancy is tuned to a specific process evolution: too much redundancy or redundancy in the wrong place wastes useful silicon area, too little redundancy also wastes die. The design optimisation means (i) takes actual defect data or randomised data for the process at the stage of evolution where the new design will enter volume production, (ii) produces graphs of every architectural variable showing revenue per wafer and yield against changes in that architectural feature.

To show the optimisation results, a parameter known as "yield" is defined as a ratio of the number of working dies to the total number of dies, and calculated as follows:

$$\text{Yield (Y)} = \frac{N_{working}}{N_{total}}\cdot 100\% = \frac{N_{perfect} + N_{recovered}}{N_{total}}\,100\% =$$

$$= \frac{P_{perf.}\,N_{tot.} + (N_{tot.} - N_{perf.})P_{recov.}}{N_{total}} = P_{perf.} + P_{recov.} - \frac{P_{perf.}\cdot P_{recov}}{100}\ \text{(in \%)},$$

where N tot. is the total number of dies;

N recov. is the number of dies recovered after laser repair;

N perf is the number of good dies before laser repair; this is constant and does not change after laser repair.

P perf. is the proportion of perfect dies compared to the total number of dies.

P recov. is the proportion of dies recovered after laser repair compared to the number of dies on which repair was attempted, i.e. **laser repair success rate.**

With respect to redundancy criteria, it should be noted that the greater the amount of redundancy, the greater the number of dies that may be repaired and the greater the yield, but the lower the total number of dies fitted on to a wafer. The memory and redundancy architectures are adjusted to obtain the minimal possible ratio of redundancy. To optimise the wafer yield by the amount of redundancy per wafer, another parameter is used, known as "revenue", which depends both on the yield and the number of dies fitted on to a wafer and is calculated as follows:

$$R = k.Y.\frac{N_{total}}{N_{wafer}} = k.\frac{N_{working}}{N_{total}}.\frac{N_{total}}{N_{wafer}} = k.\frac{N_{working}}{N_{wafer}},$$

where k is the cost parameter, e.g. market price in dollars per working die or chip or wafer,

Y is as defined above,

N_{total} is the total number of dies to be repaired,

N_{wafers} is the total number of dies per wafer.

By comparing the yield and revenue values for different memory manufacturing process variables, business information may be obtained relating to the profitability of a particular memory product manufacture. The savings that may be achieved through design optimisation are calculated on the basis of production costs, modification costs, die cost, die price, wafer cost and production capacity by the means for determining savings at design optimisation.

If an existing memory design is being run on the same process, then the design optimisation means may acquire back end test data for that memory (the memory architecture being entered into the design optimisation means before analysis), and compensate for process evolution by applying a database selection to bias the sample using anticipated defect types and densities. The actual back end test data are then highly randomised by statistical methods to alter the actual data and produce a set of data which

simulates those which may be expected for a different lot of devices to be processed, thus enabling adequate estimations of product parameters to be made.

The following input parameters may be variable in the design optimisation means: 1) the number of memory tiles per die, 2) the distribution of local and global spares against yield/wafer, 3) the quantity of each type of spare element against yield/wafer, 4) the optimal location of spares, 5) spare element size. For each variable parameter the yield and revenue graphs are plotted to define the optimal values providing the maximal yield Y (die yield) and revenue R (wafer revenue). An example flow chart of the means for estimating and enhancing revenue at design optimisation is shown in Fig. 5.

Example 1

For a given chip type BNCHMRK the following design parameters are fixed:

row bus width :12, column bus width : 12, DQ:

tile mapping: RO R1 R2 R3 R4 R5 R6 R7 R8 R9 R10 D0

C0 C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 D0,

The following parameters may be variable: the number of segments, e.g. from 2 to 128; the number of tiles per X (not more than 128); the number of tiles per Y (not more than 128); the spare row length, e.g. from 1 to 12 tiles; the spare row width, e.g. from 1 to 12 tiles; the number of shared spares, e.g. from 1 to 4; the number of spares located between segments, e.g. from 1 to 5, preferably 3; the number of global spares, from 1 to 8, preferably 4. Relative die area costs per row and column are also defined. The terms for early abort are specified as the maximum number of defects, e.g. 10,000, per die and per tile, at which the operation shall be interrupted. Full defect information about the chip under test (defect map, number of defects) is entered into the design optimisation means at the next step. Two lots of 10 and 15 chips with different defect maps are chosen for optimisation.

The optimisation of the memory design may be carried out either by tuning the chip architecture, or by tuning the redundancy type. The repair analysis is conducted sequentially for each memory device of a selected lot, information about which is stored in the database. Any suitable redundancy allocation procedure may be used to calculate the laser repair success rate, for example, well known MUST, MOST, BEST procedures or an advanced scheduled procedure described, e.g. in UK 9724529.4. To tune the chip

architecture, the wafer revenue and yield as functions of the number of memory tiles and of the tile aspect ratio are plotted, and the optimums are found for different variants. In Fig.5a the results of optimisation by tile number are shown for a lot of 10 (Lot 1) and a lot of 15 (Lot 2) BNCHMRK chips. As illustrated, the higher the number of tiles, the higher the number of chips mapped, i.e. the yield obtained, the maximum being 50% for Lot 1 and about 73% for Lot 2. However, it can be seen that the revenue calculated, taking into account the cost of each architectural variable, is not always maximal at maximum yield. Thus, for Lot 1 the revenue will be highest (about USD 730 per wafer at a price of USD 3 per good device, the average number of devices being about 500 per wafer) if the die area is divided into 128 tiles, while for Lot 2 the revenue will be highest (about USD 1600 per wafer) if the die area is divided into 8 tiles. For another tile aspect ratio, 2/1, the revenue will be maximal with the smallest number of tiles, i.e. 2 tiles, however, both the yield and revenue will be optimal at 32 tiles.

Different aspect ratios may be used when defining the redundancy architecture. In Fig.5b, yield and revenue functions obtained for a following aspect ratios: 64/2, 32/4, 16/8, 8/16, 4/32 and 2/64, are shown for Lot 1 and Lot 2 of BNCHMRK chips. As shown in Fig.5b(1) for Lot 1, the greater the difference between the number of tiles per X and the number of tiles per Y, the higher the yield and revenue obtained for the wafer. For Lot 2 (see Fig.5b(2)) of the same BNCHMRK chips, the yield is not affected by the tile aspect ratio, while the revenue is higher with a high aspect ratio, being optimal with ratios of from16/8 to 64/2..

To optimise the memory design by tuning redundancy type, the revenue and yield are plotted as a function of die level redundancy and the number of global rows and columns, for a spectrum of RA architectures.

Tuning the die level redundancy type involves modification of the number of spare columns and spare rows, the revenue and yield being plotted as functions of the number of spare columns and rows. In Fig.5c(1) yield and revenue are shown for Lot 1. As seen in the figure, revenue is greatest with the highest number of spares. In Fig.5c(2) the same graph is plotted for Lot 2; here the reverse dependence may be seen: the lower the number of spare columns, the higher the revenue obtained for the lot.

Modification of the number of global spare rows and columns for the same lots of 10 and 15 chips results in the graph shown in Fig.5d. While a standard set of 4 global

spare rows and 4 global spare columns may be used for Lot 2 of 15 BNCHMRK chips to obtain a fairly high revenue, as shown in Fig.5d(1), for Lot 1 a higher number of global spares must be used to obtain good revenues. As shown in Fig.5d(2), the revenue is far from being optimal with a standard set of global spares (from 1 to 4). By using 8 global spare columns or rows for Lot 2, the revenue may be significantly improved (up to about USD 1400 per wafer).

Optimisation may be carried out on a spectrum of redundancy architectures to obtain the most efficient solution for a given type of chip defect map and a given number of spare resources of different types: spares per tile, global spares only and both spares per tile and global spares. Different optimisation procedures may be used for performing the optimisation, e.g. the well-known dichotomy. For example, for a spectrum of RA architectures, the following revenues and yields may be obtained (see also Fig.5e):

	Yield, %		Revenue, USD	
	Lot 1	Lot 2	Lot 1	Lot 2
Spares per tile only	73.33	100	1498	1584
Global spares only	66.66	100	1482	2106
Both tiles and globals	73.33	100	1498	1584

As seen from the table, the maximum revenue may be achieved for Lot 1 (5e(1)) by using spares per tile only, while for Lot 2 the use of globals is preferable (Fig.5e(2)).

Example 2

To obtain business information, including an estimate of the actual profitability of a plant, the economic modelling means is used to calculate the actual costs and savings achieved when using the above optimisation means.

The following input information is used: the number of wafers produced in a month V = 1000, die cost D cost = 280 cents, working die price D price = 480 cents. The savings are calculated as

$$S = V[(N_{work.opt.} D_{price} - N_{total\ opt.} D_{cost}) - (N_{work\ org.} D_{price} - N_{total\ org.} D_{cost})].$$

	Original Design	Optimised Design (I)	Optimised Design (II)
Number of dies fitted on to a wafer	508	498	499
Percentage of perfect die	5	5	5
Laser repair success rate, %	50	96	73,33
Increase in yield, %		79,63	39,70
Savings, USD/month .1000 wafers		424,752	211,77

The means for estimating and enhancing revenues at wafer probe test optimisation includes a test optimisation means for identifying the optimum defect coverage for given die, probe, yield and back end processing costs; modification of tests to achieve this with the minimum ATE time; and a means for calculating the savings achieved using the optimised or reduced test sequence The flow chart of the means for estimating and enhancing profits at wafer test optimisation is shown in Fig. 6.

The first step is to determine exactly what coverage the wafer probe tests are actually achieving. This is done by using statistical information about the defects, represented in the form of a defect map and a list sequence of tests that cover this type of defect. The quickest way of achieving this is to test partial DRAMs as packaged parts using conventional emulation pods or pods specially designed for this purpose. If packaged partials are not available, then the total coverage can be estimated by acquiring fail data from the wafer probe ATE running the wafer probe sequence, then using the test sequence optimisation means proposed in UK 9716812.4 to determine the coverage over time, and then extrapolating the coverage asymptote.

The second step, after the total number and type of defects has been ascertained using standard test equipment or the test optimisation means specially adapted for the purpose, is to determine the coverage achieved in each test in the wafer test sequence. The best way to do this is to run the wafer sequence on the same packaged partials used to determine the coverage. If this is not possible, then similar information can be obtained statistically from data gathered in wafer probe; however, much more data will be required.

It is essential to note that using packaged partials to optimise the wafer probe sequence is possible in most cases. After burn-in, partials have the same defect types as at wafer probe unless the spares are tested at wafer probe, but the distribution is skewed with far fewer gross defects. The gross defects are not of interest, as any competent test should find them.

The wafer probe test sequence obtained is then optimised for coverage over time. This is achieved by using the test optimisation means. The operation of the test optimisation means is described in UK 9716812.4 which is incorporated herein by reference. Any other suitable test optimisation may be carried out, e.g. that described in US 4875002. The next step is building a model of the business economics to determine what is the optimal cut-off point for wafer probe. Optimal overall business profitability

may be achieved when a wafer probe test sequence does not have 100% coverage - the wafer probe test should not attempt to do the job of final packaged test, which must have better than 1-30 PPM coverage. This business calculation compensates for the yield differences, burn in costs, packaging costs and final test costs. The test sequence may be interrupted, i.e. cut-off, e.g. at coverages of 85-99%. In Fig.7 the test sequence is cut off at a coverage of about 93%.

Finally, compensation for the differences between wafer probe fault distribution and final test fault distribution is carried out. This compensation is achieved by comparing the performance in terms of coverage over time for the optimised wafer probe sequence and the original one by acquiring data from the wafer probe ATE. This step is needed to accommodate particular defect types whose distribution is skewed by the laser repair process.

On the basis of this information the economic modelling means calculates the possible savings that may be obtained by using the optimised test sequence at a fixed yield.

Example 3

The profits that may be obtained using different wafer probe test sequences are compared for a lot of 118 chips type MIC4MX4 (Micron 16 Mb EDO DRAM, 2K refresh, 4DQs, 5V) tested on Megatest Genesis G2). The optimisation is carried out for a standard test combination of 79 tests. To maximise defect coverage as early as possible, the optimal test sequence is found by determining the coverage achieved by each test in the combination and the overall coverage for the test sequence. The results obtained for different coverages are compared to obtain maximum coverage in minimum time.

Total number of tests in original sequence: 79.

Optimisation methods performed: - maximizing the percentage increase procedure
- minimizing the redundancy procedure
- selecting the best adjusted test procedure.

Number of tests in the optimised sequence: 46

Overall optimised sequence:

Coverage, %	Test
86.948692	EMULRE3C
93.764549	HPMARC3
95.922562	EMULRE1B

```
97.707596   CDISTH
98.197433   MARC6
98.491531   EMULRE1B
98.771019   CDIST
99.025192   MARC3
99.206329   LONGDEL
99.334869   RDIST2H
99.442970   PMARC3
99.536453   EMULRE2
99.628967   EMULRE4C
99.688370   HPMARC1
99.741936   PMARC2
99.784782   CDISTF
99.820816   MARC1
99.851974   EMULRE2
99.868530   RDIST2E
99.884117   EMULRE2B
99.898720   EMULRE1C
99.911385   SREC
99.923065   EMULRE9C
99.932808   EMULRE2A
99.942543   EMULRE1A
99.950333   EMULRE2C
99.956177   CDIST2A
99.962021   EMULRE4B
99.967865   EMULRE2
99.972733   RDIST2C
99.976631   EMULRE7C
99.979553   CDIST
99.982468   CDIST
99.984421   PMARC3
99.986366   RDIST2D
99.988312   RDIST2A
99.990265   CDISTC
99.992210   EMULRE8C
99.993187   PMARC1
99.994156   RDIST2B
99.995132   RDIST2C
99.996101   RDIST2D
99.997078   CDIST2F
99.998055   CDIST2G
99.999023   CDIST2G
100.000000  EMULRE3B
Original sequence execution time:    90.00
Optimised sequence execution time:    3.91
Percentage of time reduction:        95.65
```

On the basis of the above optimisation, the following business calculation is carried out.

Number of wafers produced per month	1000
Processing (test, burn-in, packaging) costs, cents	180
Number of die on a wafer	400
Wafer probe cost/device.second	2
% of defective die	40
Wafer coverage (defect PPM)	100
Wafer probe time, seconds	90
Reduced probe time:	3.91

Reducing probe time to 3.91 seconds will reduce coverage by 9 PPM, saving 172.17 cents on wafer probe test but increasing back end costs by 0.0016 and reducing yield by typically 0.00090%. In this case the overall operational savings would be 660.915 USD/month .1000 wafers. The wafer probe test savings may be calculated as follows:

$$S = N_{def.die}\, T_{cost}\, (t_{orig} - t_{red}) - D_{cost}\, (N_{def.\ die\ red.} - N_{def.die}) =$$

$$= N_{die}[C_{orig} T_{cost}\, (t_{orig} - t_{red}) - D_{cost}(C_{red} - C_{orig})]$$

Where $N_{def.\ die}$ is the number of defect dies found in a wafer probe test which is calculated as $N_{def.\ die} = N_{die} \cdot C_{orig}$,

where C_{orig} is test coverage, in defect die PPM, achieved by original test sequence, $N_{def\ die\ red} = N_{die} \cdot C_{red}$,

where C_{red} is test coverage, in defect die PPM, achieved by a reduced test sequence,

T_{cost} is the test time cost in cents per device and per second.

t_{orig} is original test time,

t_{opt} is optimised test time.

The means for estimating and enhancing revenues at laser repair optimisation is adapted to maximise yield recovery as a function of resource cost, die cost and die characteristics, by comparing different redundancy allocation algorithms, and thus to increase business revenues.

To chart the yield differences from different redundancy allocation algorithms, any suitable design optimisation means may be used, for example, the design optimisation means proposed in the present invention. The design optimisation means has accurate

models for all major redundancy allocation hardware and software. This allows redundancy procedures to be compared for yield and recovery ratio on a batch of die. Using some of the known design optimisation means, the maximum batch size is 200 die. Using the design optimisation means proposed in the present invention, the maximum batch size which can be stored on a single disk is 16,000,000.

The flow chart of the means for estimating and enhancing revenues at laser repair optimisation is shown in Fig.8. To optimise business parameters by tuning redundancy allocation (RA) procedures, the results obtained for a given actual defect map and chip type by different available allocation procedures, for example, MUST, MOST, BEST and Scheduled, may be calculated and compared. For the above lot of 10 chips, type BNCHMRK, the yield will be 10.00% for MUST, 40.00% for MOST RA procedures at die level, and 80.00% for BEST and Scheduled RA procedures respectively (see Fig.8a1). For the above lot of 15 chips, the yield will be 85,6% for MOST, BEST and Scheduled RA procedures and 11% for MUST (see Fig.8b). The order of spares, module architecture and RA restrictions are fixed for both lots.

The means for estimating and enhancing revenues at package test optimisation is adapted for maximising coverage as a function of time and enhancing the possible business profits. The flow chart of the means for estimating and enhancing profitability at packaged part test optimisation is shown in Fig. 9.

The first step is to determine exactly what coverage the packaged part tests are actually achieving. The quickest way of achieving this is to test partial DRAMs as packaged parts using the environment emulation pods described, e.g. in UK 9714130. If the packaged partials are not available, then the total coverage can be estimated by acquiring fail data from package ATE running the package sequence, then using the means for test sequence optimisation proposed in the present invention to determine the coverage over time, and then extrapolating the coverage asymptote.

The second step, after the total number and type of defects has been ascertained using the test optimisation means, is to determine the coverage of each test in the package test sequence. The best way to do this is to run the package sequence on the same packaged partials used to determine the coverage.

The third step is optimising the package sequence for coverage over time by using

the test optimisation means in accordance with the present invention

On the basis of the above optimisation, a model of the business economics is built to determine what savings can be achieved by using the test optimisation means proposed in the present invention. This business calculation compensates for the final test costs. Operational savings in this case may be calculated as follows:

$$S = N_{die} (t_{test} - opt\ t_{test}) \cdot Test_{cost}$$

For example, for a lot of 118 MIC4MX4 chips the following parameters are used:

Number of devices tested per month	60,000,000
Device package test cost (per device.second), cents	0.75
Original test time, sec	240
Percentage of time reduction obtained by using test optimisation means	41.77
Reduced test time, s	139.75

As calculated above, operational savings would be USD 4,511,392 per month.

The means for estimating and enhancing revenues by modifying the device compatibility is adapted for estimating the compatibility of the memory device product with particular motherboards to produce a compatibility list and calculating the possible savings and revenues achieved if the customised product is produced according to this compatibility list.

The means for modifying compatibility predicts which applications will cause the product to fail and recommends changes to the design, processing or, usually, test to achieve maximum compatibility. The flow chart of the means for estimating and enhancing profitability by modifying compatibility is shown in Fig.10.

To get the compatibility information, the parameters of particular motherboards are captured and reproduced on application pods. Any suitable application pods, including emulators or engineering testers specially developed for this purpose, some low cost testers or, alternatively, the means for measuring data strobe may be used.

Thus, the application pods are preconfigured with the full parametric, timing and functional characteristics of a wide range of motherboards and Original Equipment Manufacturer (OEM) acceptance tests, and a representative set of good devices, preferably more than 1000 devices, is assembled into these application pods and retested in the emulated environment.

Compatibility is estimated based on the timing characteristics, including data strobe, used in the motherboards of a spectrum of manufacturers. To measure this strobe, a special test hardware board, described in UK 9714130, is used. If the application is not currently emulated in the application pod or low cost tester used, then the data strobe timing, as well as the signals, which can be observed directly, may be measured using this special test hardware board. The timing characteristics obtained are entered as a new timing set.

The test results are analyzed, for example, by plotting a Schmoo plot, and a set of motherboards compatible with the given memory type is determined to produce the compatibility list. The savings that may be achieved are calculated by a means for determining savings at maximal compatibility. The revenues achieved in this case take into account both the increased end value of the device and the costs of increased test time as follows:

$$S = D_{cost2} \cdot N_{2product} - D_{cost1} \cdot N_{1product} - N_{2product} (t_2 - t_1) \cdot T_{cost}$$

Where D_{1cost} ($) is the market price for an original chip or wafer product,
D_{2cost}($) is the market price for a customised chip or wafer product,
$N_{product}$ is the number of chips sold at an increased price.
T_{cost} is the test time cost in cents per device and per second
t_1 is original test time, t_2 is increased test time.

The means disclosed above, are preferably implemented in hardware, but may also be embodied in a software program stored in an electrically readable media.

It will be appreciated that the above are example embodiments only and that various modifications may be made to the embodiments described above within the scope of the present invention.

CLAIMS

1. A system for modelling memory business parameters using back end test data and a structural description of the memory device stored in a database, ***characterised in that*** the system contains a plurality of economic modelling means for profiling and modelling the economic parameters of the memory business.

2. The system according to claim 1, ***characterised in that*** the system further includes a randomisation means for statistical randomisation of the actual back end test data.

3. The system according to claims 1-2, ***characterised in that*** the plurality of economic modelling means consists of a plurality of engineering modification means and a plurality of means for determining savings.

4. The system according to claims 1-3, ***characterised in that*** the plurality of economic modelling means comprises at least one means selected from a means for estimating and enhancing revenue by yield optimisation, a means for estimating and enhancing revenue by test optimisation, and a means for estimating and enhancing revenue by improving compatibility.

5. The system according to claims 1-4, ***characterised in that*** each economic modelling means comprises a corresponding modification means provided with a corresponding means for determining savings.

6. The system according to claims 4-5, ***characterised in that*** the means for estimating and enhancing revenue by optimisation of the yield in terms of finished good devices as a function of the cost of sales contains at least one means selected from a means for estimating and enhancing revenue at design optimisation and a means for estimating and enhancing revenue at laser repair process optimisation.

7. The system according to claims 4-6, ***characterised in that*** the means for estimating and enhancing revenue by test optimisation contains at least one means selected from a means for estimating and enhancing revenue at wafer probe test optimisation and a means for estimating and enhancing revenue at package test optimisation.

8. The system according to claims 4-7, ***characterised in that*** the means for estimating and enhancing revenue by improving compatibility contains at least one means selected from a means for estimating and enhancing revenue by modifying the device specification. a means for estimating and enhancing revenue by modifying compatibility

and a means for estimating and enhancing revenue at incoming inspection by the end user or buyer.

9. The system according to claim 8, ***characterised in that*** the means for estimating and enhancing revenue by modifying the device specification includes:

a means for issuing a detailed application report for each market segment specifying the variance with a worst case DRAM datasheet,

a means for collecting the defect information for each worst-case requirement application configured on an application pod,

a means for correlating production chip results with the results obtained from the application pod,

a means for analysing timings, voltage and refresh rates for tests on the application pod to determine the particular parameter values which cause device failures,

a means for determining savings achieved by using the modified specification.

10. The system according to claims 4-9, ***characterised in that*** the means for estimating and enhancing revenue by yield optimisation includes:

a means for obtaining defect data for the process,

a means for randomisation of the actual defect data to produce a set of data expected at a future evolutionary step in process development,

a means for producing graphs of architectural variables showing revenue per wafer and yield against changes in an architectural feature,

a means for determining savings defined as the difference between revenues and costs at original and optimal design.

11. The system according to claim 10, ***characterised in that*** the means for obtaining defect data acquires back end test data for an existing memory design entered before analysis and compensates for process evolution by applying a database selection to bias the sample using anticipated defect types and densities.

12. The system according to claims 10-11, ***characterised in that*** the means for producing graphs uses at least one of the following parameters: the number of memory tiles, the number of spares, the distribution of local and global spares against revenue per wafer, the quantity of each spare resource against revenue per wafer, the optimal location of spares.

13. The system according to claims 4-12, ***characterised in that*** the means for estimating and enhancing revenue by test optimisation includes:

a means for determining the coverage achieved by a particular test in a sequence,

a means for determining the total coverage achieved by the test sequence, and

a means for determining the optimal test sequence having a maximal coverage, and

a means for calculating the savings achieved by using the optimised test sequence.

14. The system according to claims 4-13, ***characterised in that*** the means for estimating and enhancing revenue at wafer test optimisation uses data obtained at packaged part testing.

15. The system according to claims 4-14, ***characterised in that*** the means for estimating and enhancing revenue by test optimisation further includes a means for calculating the savings achieved by using a wafer probe test sequence interrupted at an optimal point in time, the savings being calculated on the basis of financial factors, such as test time savings, yield effects in later stages, the number of finished goods, and others, such as the increase of test time caused by defective devices being permitted to continue in the process flow.

16. The system according to claims 4-15, ***characterised in that*** the means for estimating and enhancing revenue at laser repair optimisation comprises

a laser repair optimisation means for comparative analysis of different redundancy procedures, and

a means for determining savings at laser repair optimisation using yield data for different redundancy procedures.

17. The system according to claims 4-16, ***characterised in that*** the means for estimating and enhancing revenue by modifying compatibility comprises a compatibility modelling means including a means for measuring the data strobes generated by motherboards produced by different manufactures, a means for reproducing different motherboard parameters and retesting memory devices, a means for analysing test results to produce a compatibility list, and a means for determining savings at maximal compatibility.

18. A method of modelling a memory device business using back end test data and a structural description of the memory device stored in a database, the method including at least one economic modelling step for profiling and modelling the economic performance of the memory business using the system according to any one of claims 1-17.

19. The method according to claim 18, ***characterised in that*** the economic modelling steps includes at least one step for estimating and enhancing the profitability of a memory industry plant selected from a step of estimating and enhancing the revenue by yield optimisation, a step of estimating and enhancing profits by test optimisation and a step of estimating and enhancing the revenue by improving compatibility.

20. The method according to claims 18-19, ***characterised in that*** the method further includes at least one engineering modification step for modification and/or optimisation of engineering criteria.

21. A computer implemented method for profiling and modelling the economic performance of the memory business using the system according to claims 1-17 and/or a method according to claims 18-20.

22. A computer aided design device for profiling and modelling the economic performance of the memory business using the system according to claims 1-17 or a method according to claims 18-21.

23. A computer readable memory operable in a computer aided design apparatus according to claim 22, the computer readable memory comprising a computer program for performing a computer implemented method according to claim 21.

24. A computer program for implementing or emulating or simulating the hardware functions of a system, device or method as claimed in any one of claims 1-22 when stored in electrically readable media.

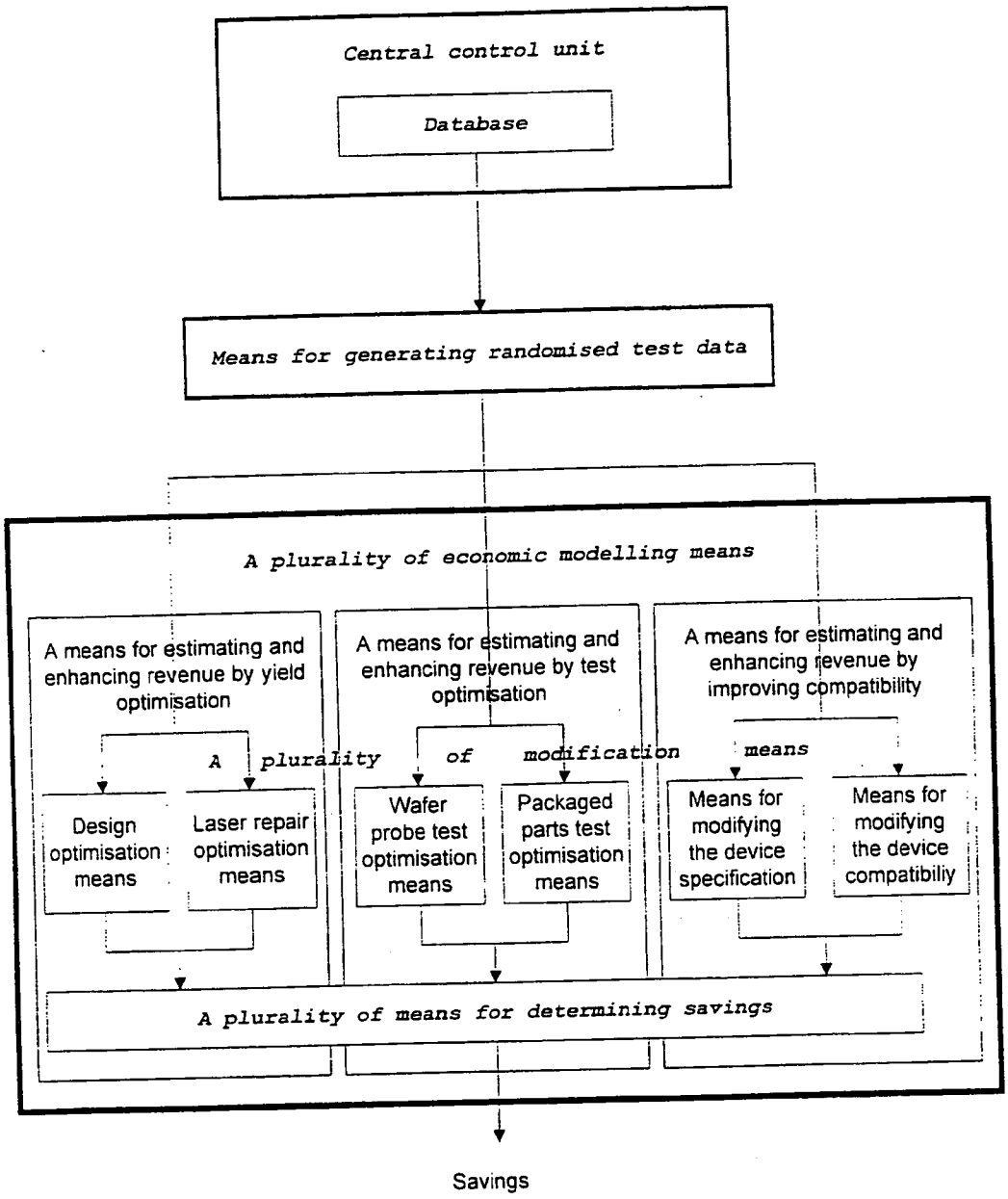
Central control unit
Database
Means for generating randomised test data
A plurality of economic modelling means
A means for estimating and enhancing revenue by yield optimisation
A means for estimating and enhancing revenue by test optimisation
A means for estimating and enhancing revenue by improving compatibility
A plurality of modification means
Design optimisation means
Laser repair optimisation means
Wafer probe test optimisation means
Packaged parts test optimisation means
Means for modifying the device specification
Means for modifying the device compatibiliy
A plurality of means for determining savings
Savings

Fig.1

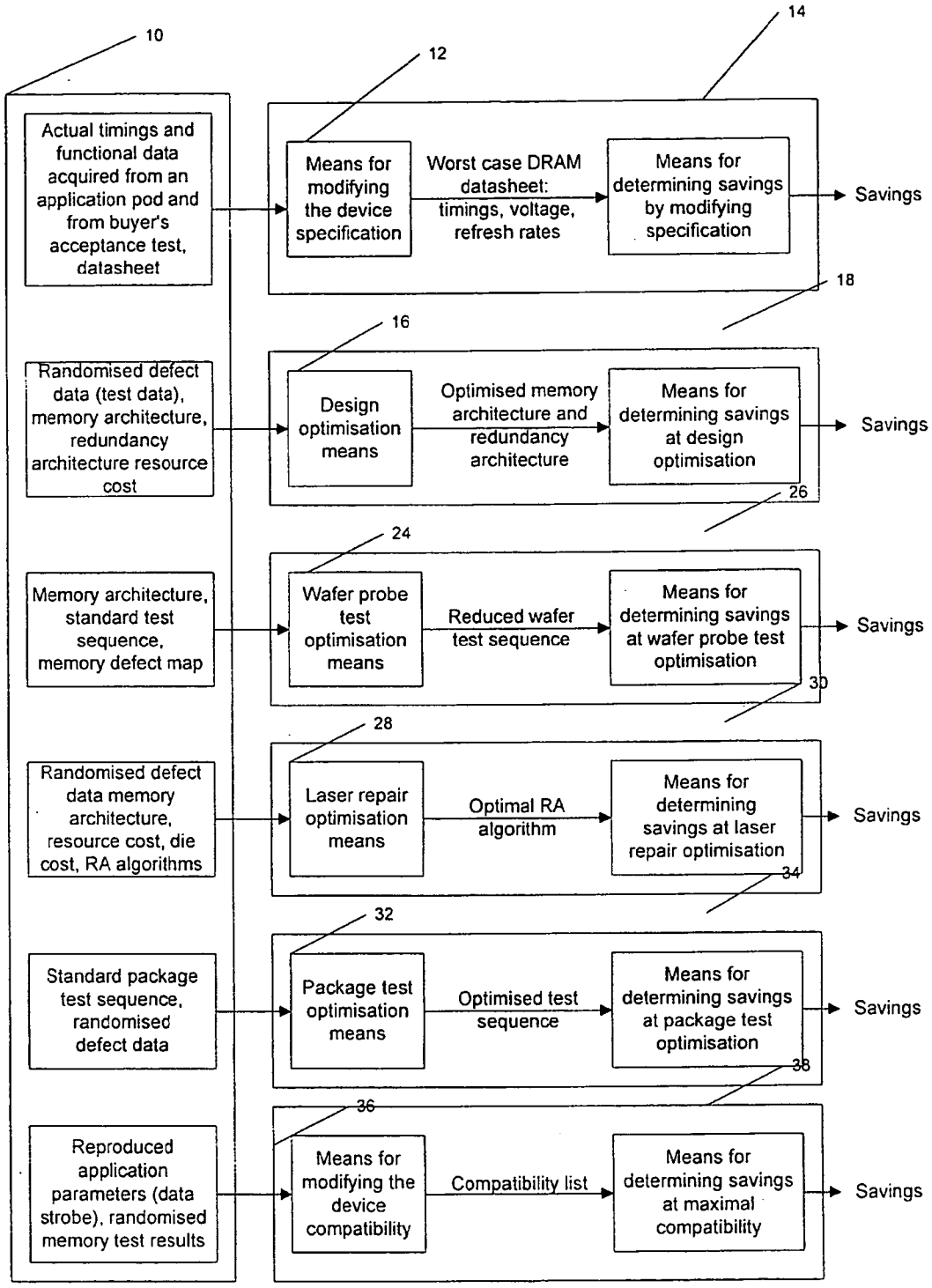
10
12
14
Actual timings and functional data acquired from an application pod and from buyer's acceptance test, datasheet
Means for modifying the device specification
Worst case DRAM datasheet: timings, voltage, refresh rates
Means for determining savings by modifying specification
Savings
18
16
Randomised defect data (test data), memory architecture, redundancy architecture resource cost
Design optimisation means
Optimised memory architecture and redundancy architecture
Means for determining savings at design optimisation
Savings
26
24
Memory architecture, standard test sequence, memory defect map
Wafer probe test optimisation means
Reduced wafer test sequence
Means for determining savings at wafer probe test optimisation
Savings
30
28
Randomised defect data memory architecture, resource cost, die cost, RA algorithms
Laser repair optimisation means
Optimal RA algorithm
Means for determining savings at laser repair optimisation
Savings
34
32
Standard package test sequence, randomised defect data
Package test optimisation means
Optimised test sequence
Means for determining savings at package test optimisation
Savings
38
36
Reproduced application parameters (data strobe), randomised memory test results
Means for modifying the device compatibility
Compatibility list
Means for determining savings at maximal compatibility
Savings

Fig.2

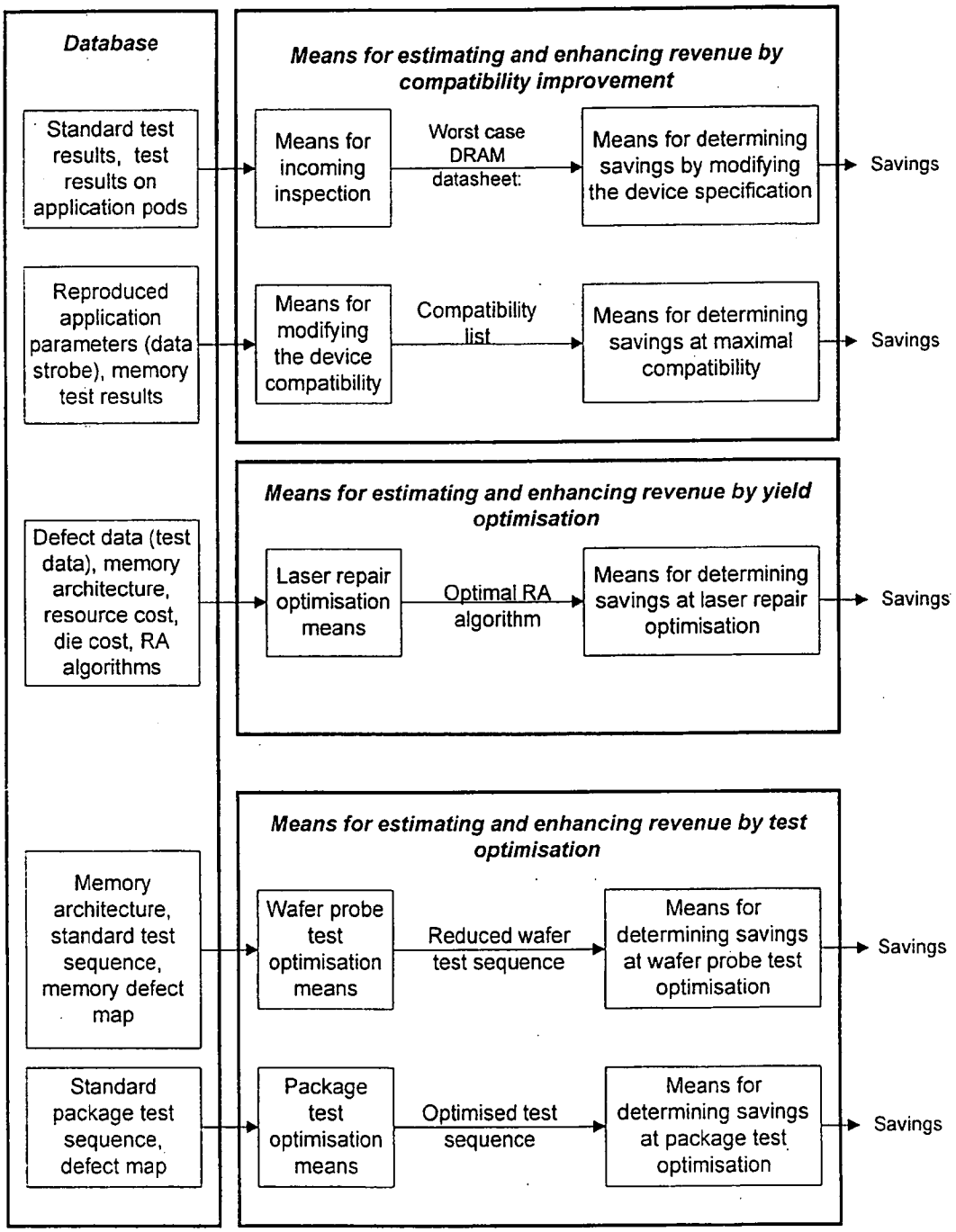
Database
Standard test results, test results on application pods
Reproduced application parameters (data strobe), memory test results
Defect data (test data), memory architecture, resource cost, die cost, RA algorithms
Memory architecture, standard test sequence, memory defect map
Standard package test sequence, defect map
Means for estimating and enhancing revenue by compatibility improvement
Means for incoming inspection
Worst case DRAM datasheet:
Means for determining savings by modifying the device specification
Savings
Means for modifying the device compatibility
Compatibility list
Means for determining savings at maximal compatibility
Savings
Means for estimating and enhancing revenue by yield optimisation
Laser repair optimisation means
Optimal RA algorithm
Means for determining savings at laser repair optimisation
Savings
Means for estimating and enhancing revenue by test optimisation
Wafer probe test optimisation means
Reduced wafer test sequence
Means for determining savings at wafer probe test optimisation
Savings
Package test optimisation means
Optimised test sequence
Means for determining savings at package test optimisation
Savings

Fig.3

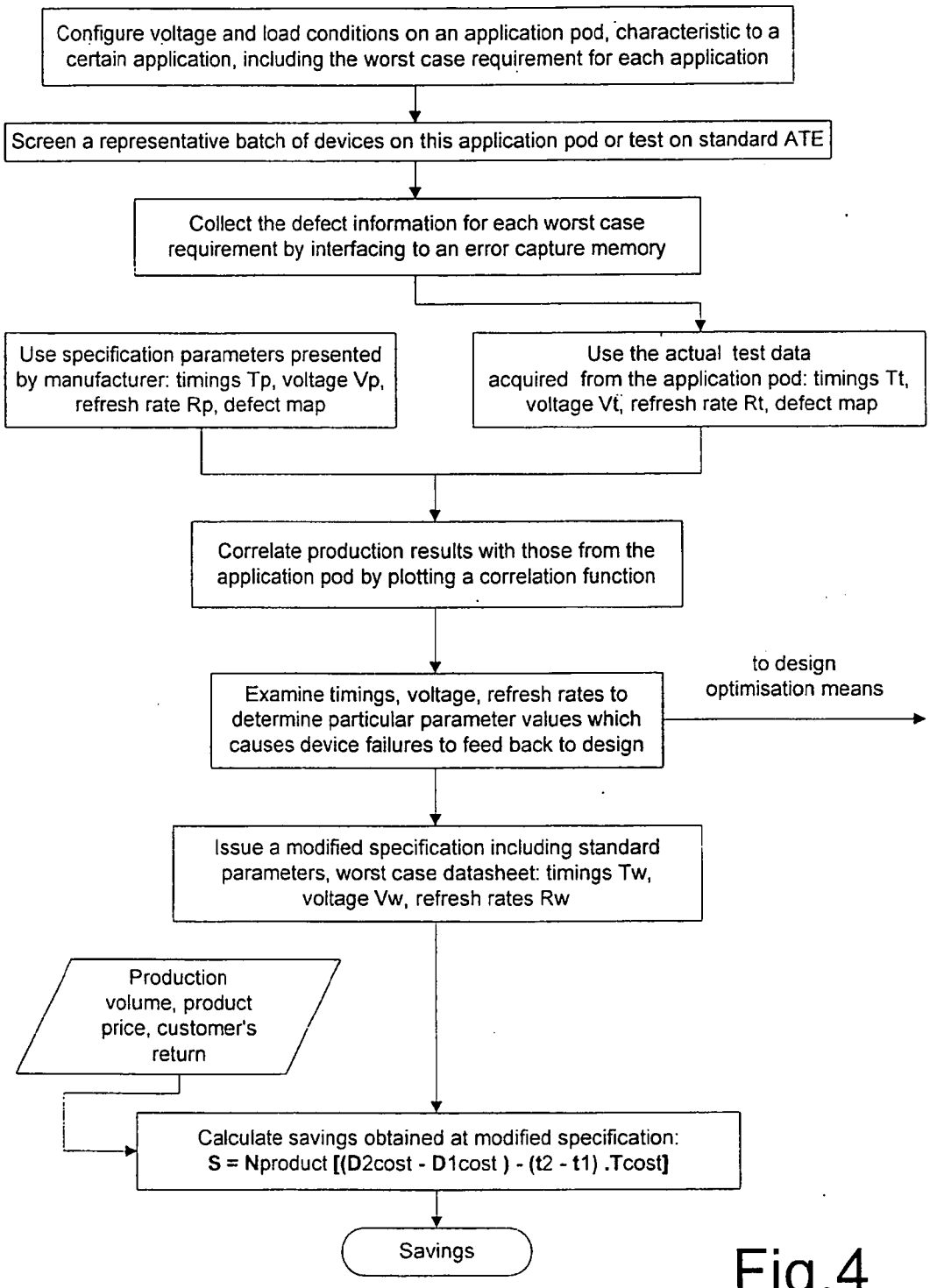
Configure voltage and load conditions on an application pod, characteristic to a certain application, including the worst case requirement for each application
Screen a representative batch of devices on this application pod or test on standard ATE
Collect the defect information for each worst case requirement by interfacing to an error capture memory
Use specification parameters presented by manufacturer: timings Tp, voltage Vp, refresh rate Rp, defect map
Use the actual test data acquired from the application pod: timings Tt, voltage Vt, refresh rate Rt, defect map
Correlate production results with those from the application pod by plotting a correlation function
Examine timings, voltage, refresh rates to determine particular parameter values which causes device failures to feed back to design
to design optimisation means
Issue a modified specification including standard parameters, worst case datasheet: timings Tw, voltage Vw, refresh rates Rw
Production volume, product price, customer's return
Calculate savings obtained at modified specification:
S = Nproduct [(D2cost - D1cost) - (t2 - t1) .Tcost]
Savings

Fig.4

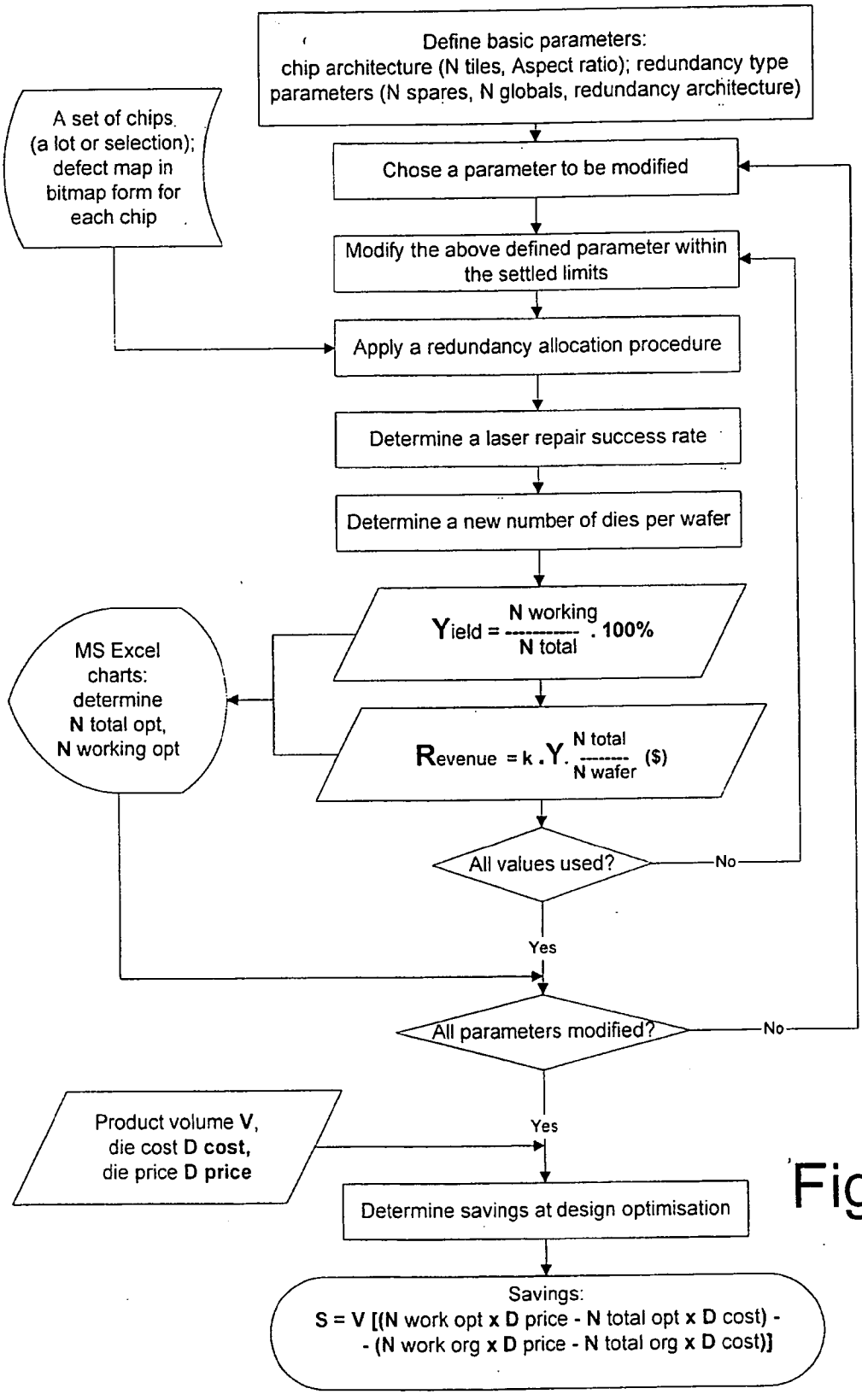
Define basic parameters:
chip architecture (N tiles, Aspect ratio); redundancy type parameters (N spares, N globals, redundancy architecture)
A set of chips. (a lot or selection); defect map in bitmap form for each chip
Chose a parameter to be modified
Modify the above defined parameter within the settled limits
Apply a redundancy allocation procedure
Determine a laser repair success rate
Determine a new number of dies per wafer
Yield = N working / N total . 100%
MS Excel charts: determine N total opt, N working opt
Revenue = k . Y . N total / N wafer ($)
All values used?
No
Yes
All parameters modified?
No
Yes
Product volume V, die cost D cost, die price D price
Determine savings at design optimisation
Savings:
S = V [(N work opt x D price - N total opt x D cost) -
- (N work org x D price - N total org x D cost)]

Fig.5

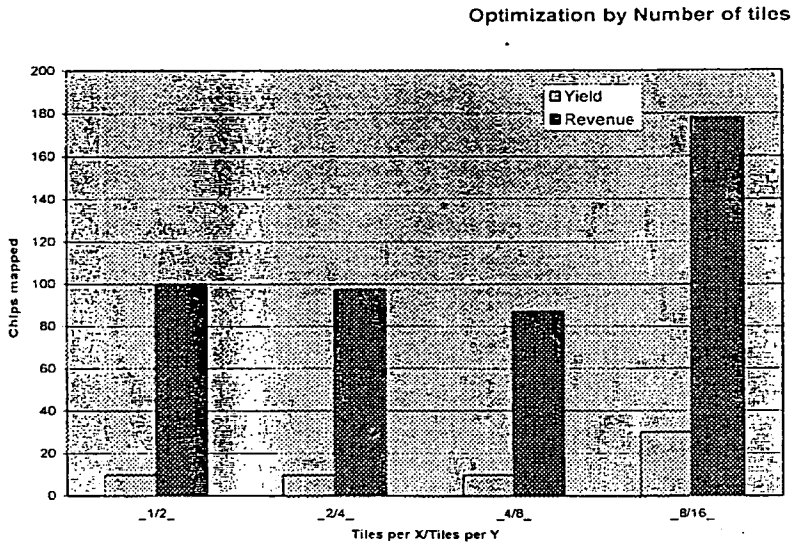

Fig.5a(1)

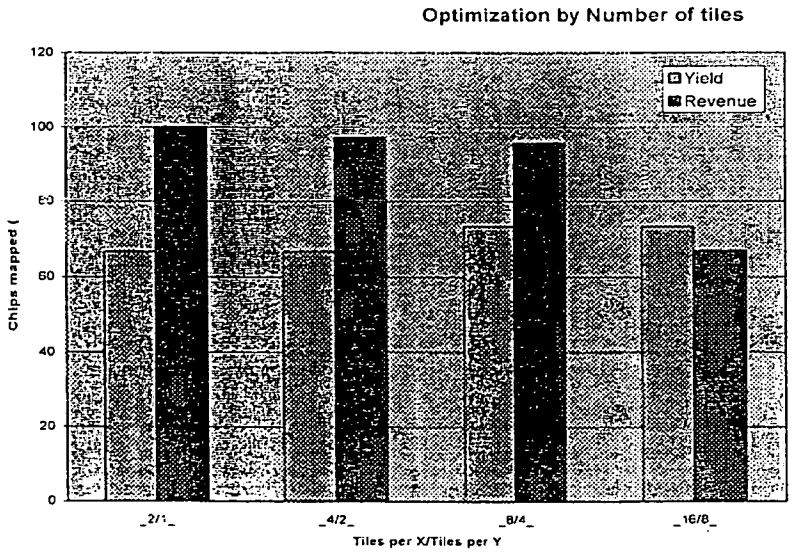

Fig.5a(2)

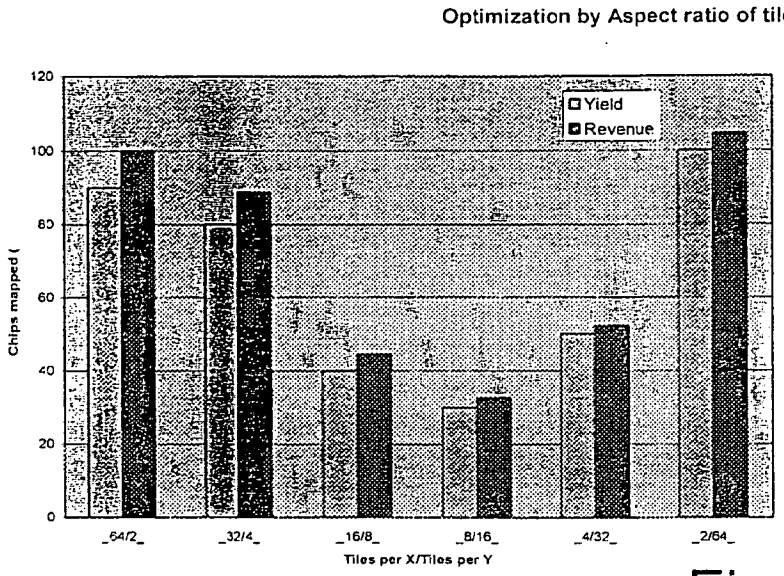

Fig.5b(1)

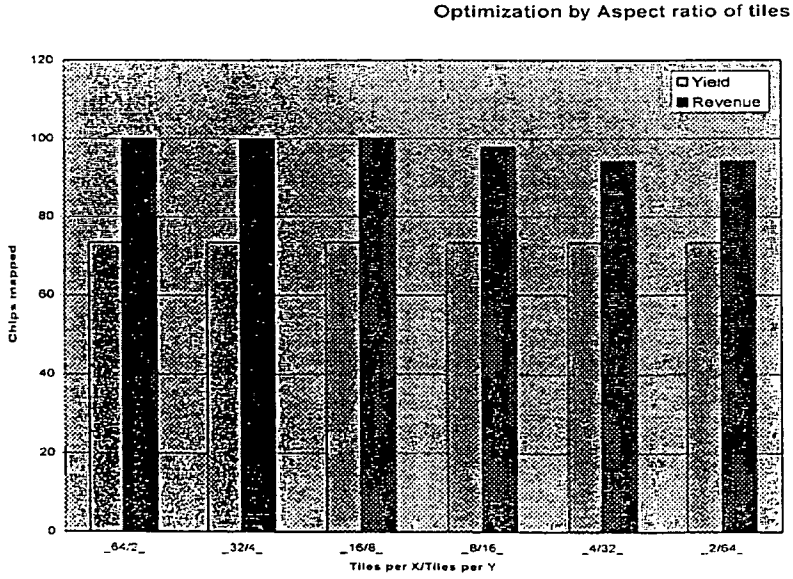

Fig.5b(2)

Optimization of the number of spares for each tile, using Domain-Region Model

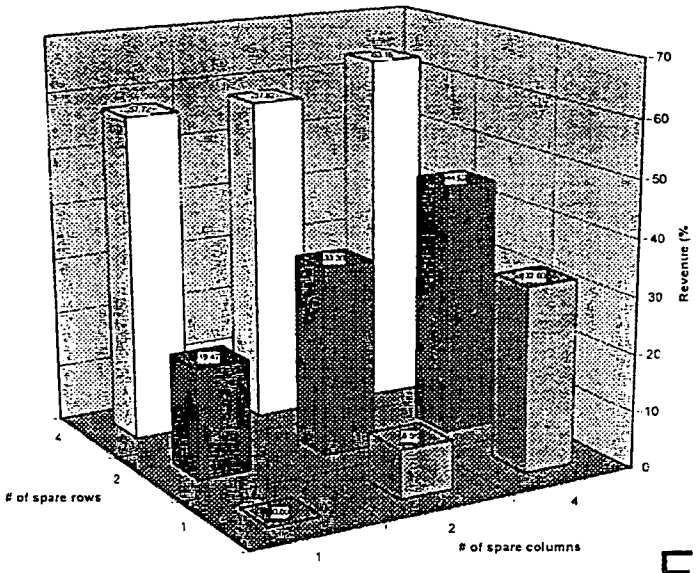

Fig.5c(1)

Optimization of the number of spares for each tile, using Domain-Region Model

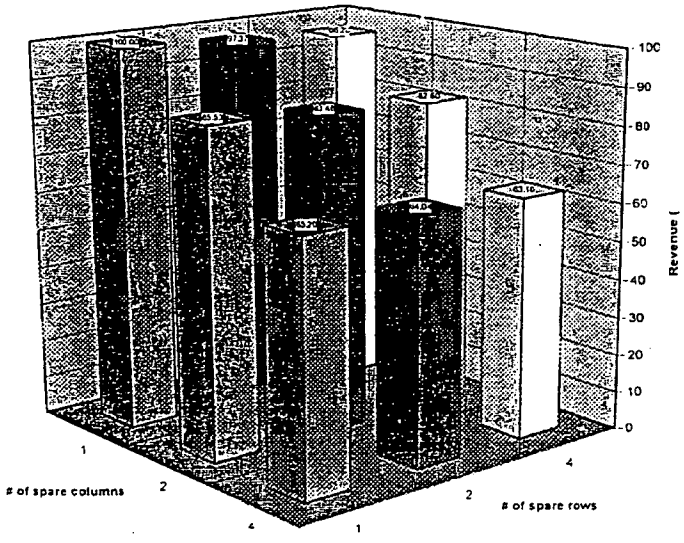

Fig.5c(2)

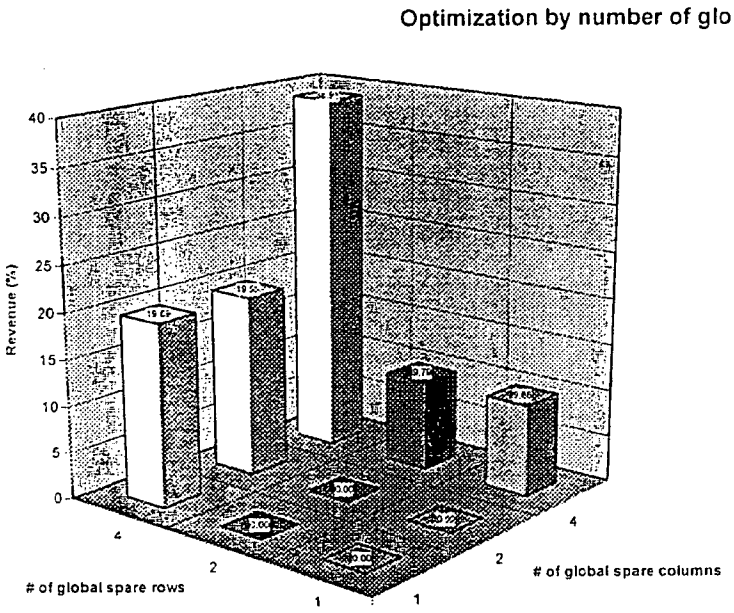

Fig.5d(1)

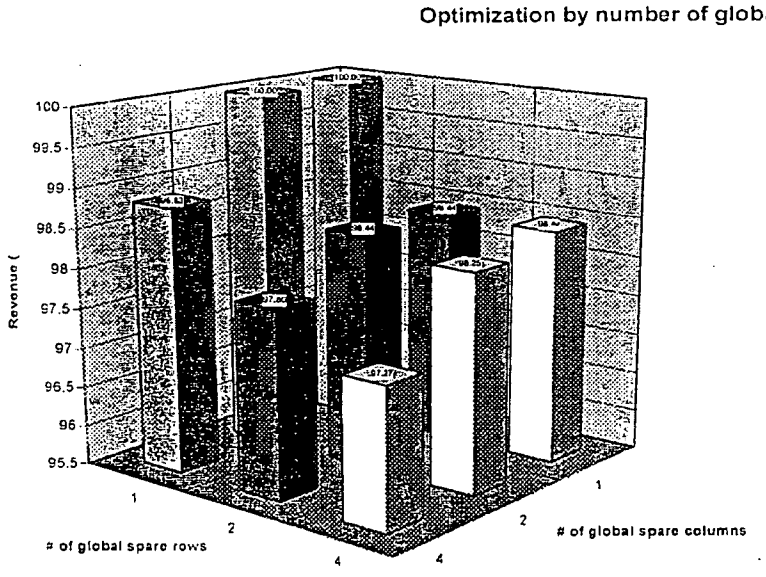

Fig.5d(2)

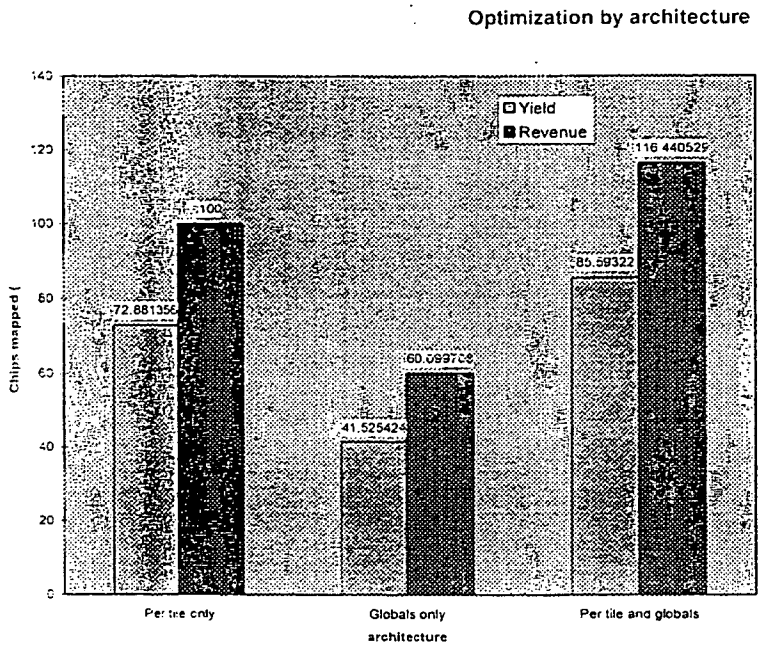

Fig.5e(1)

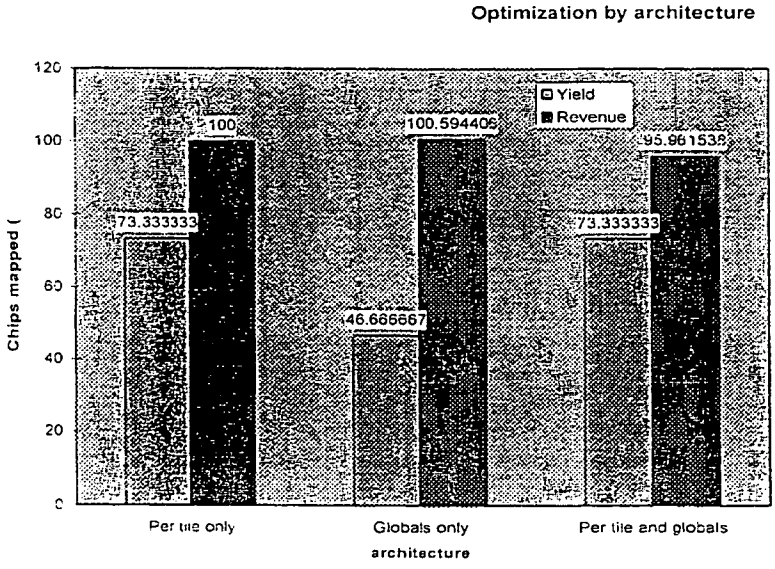

Fig.5e(2)

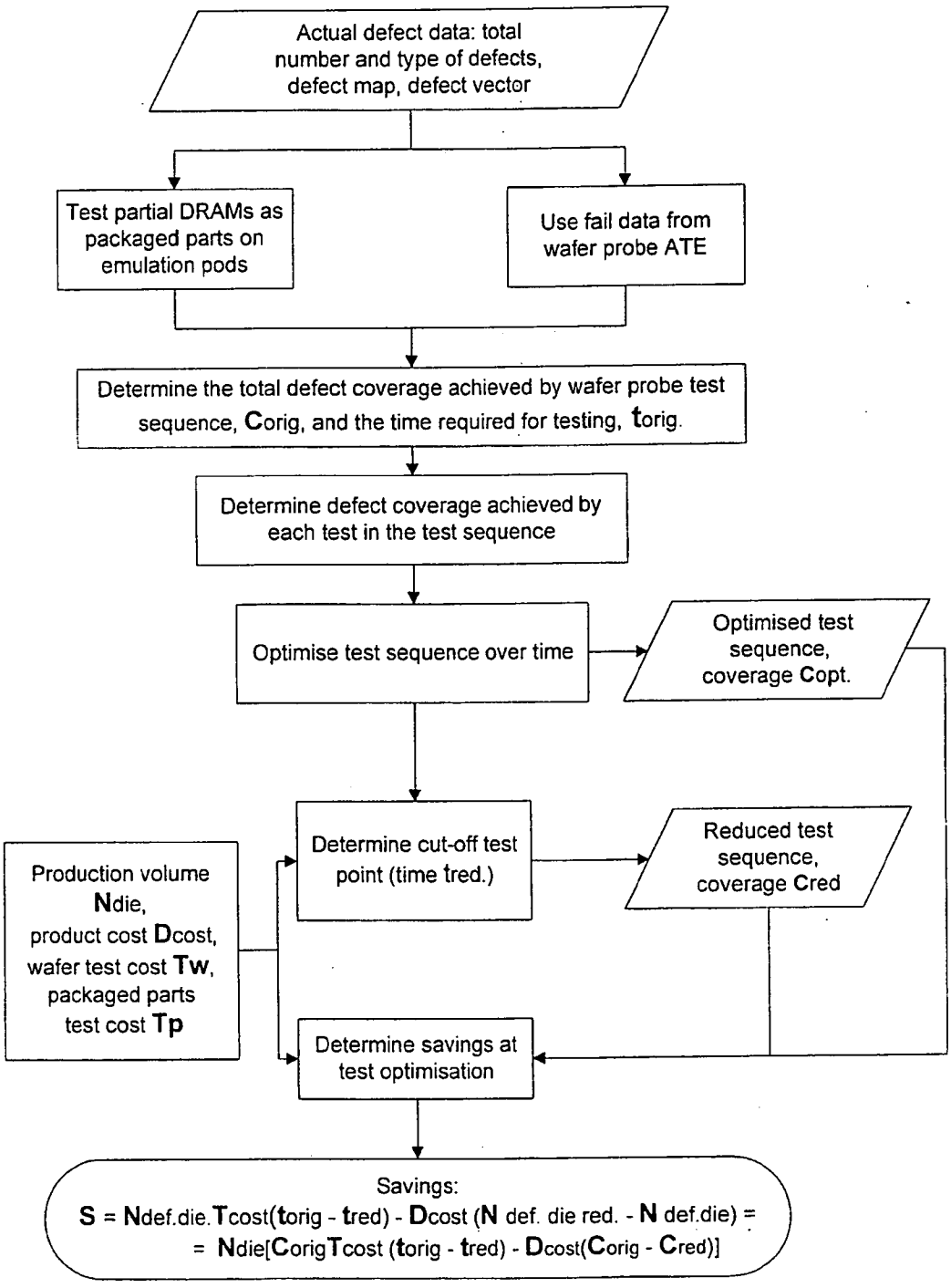
Actual defect data: total number and type of defects, defect map, defect vector
Test partial DRAMs as packaged parts on emulation pods
Use fail data from wafer probe ATE
Determine the total defect coverage achieved by wafer probe test sequence, Corig, and the time required for testing, torig.
Determine defect coverage achieved by each test in the test sequence
Optimise test sequence over time
Optimised test sequence, coverage Copt.
Production volume Ndie, product cost Dcost, wafer test cost Tw, packaged parts test cost Tp
Determine cut-off test point (time tred.)
Reduced test sequence, coverage Cred
Determine savings at test optimisation
Savings:
S = Ndef.die.Tcost(torig - tred) - Dcost (N def. die red. - N def.die) =
= Ndie[CorigTcost (torig - tred) - Dcost(Corig - Cred)]

Fig.6

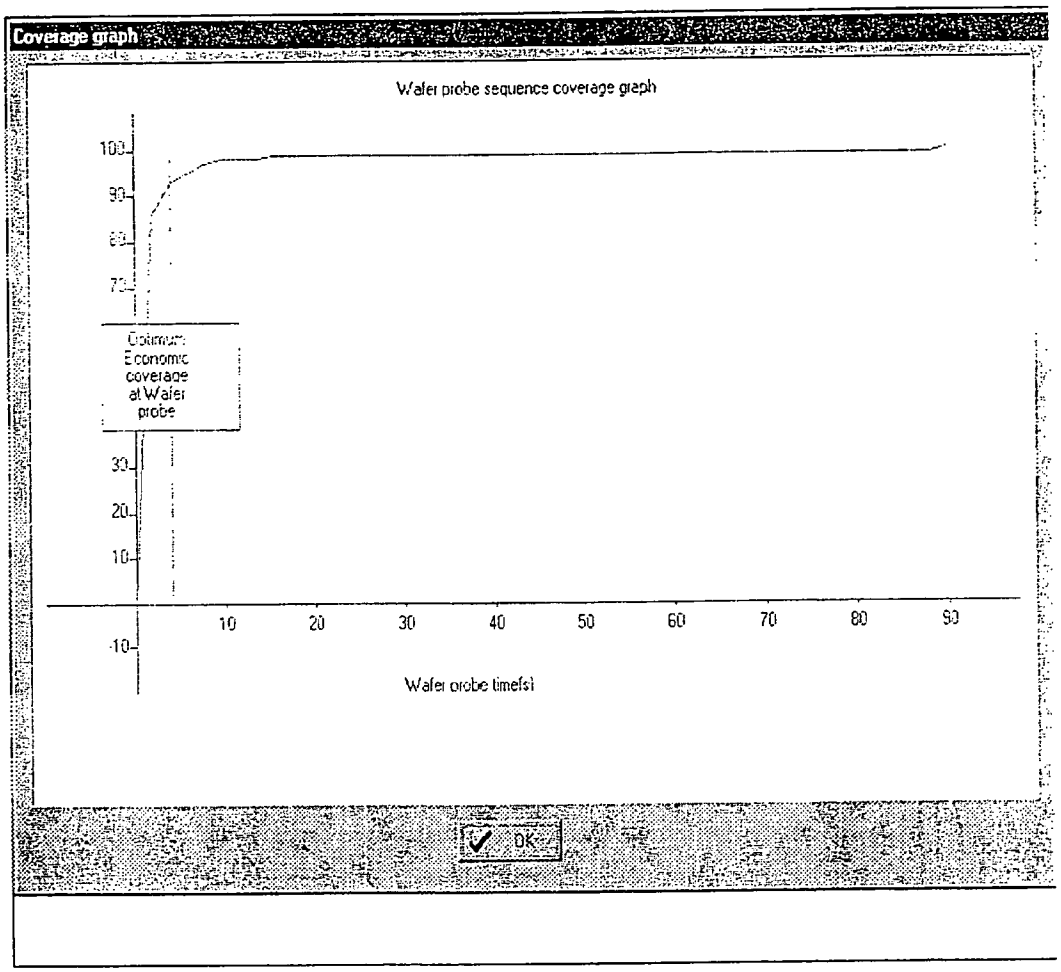
Coverage graph
Wafer probe sequence coverage graph
100
90
80
70
Optimum Economic coverage at Wafer probe
30
20
10
-10
10
20
30
40
50
60
70
80
90
Wafer probe timefs)
OK

Fig.7

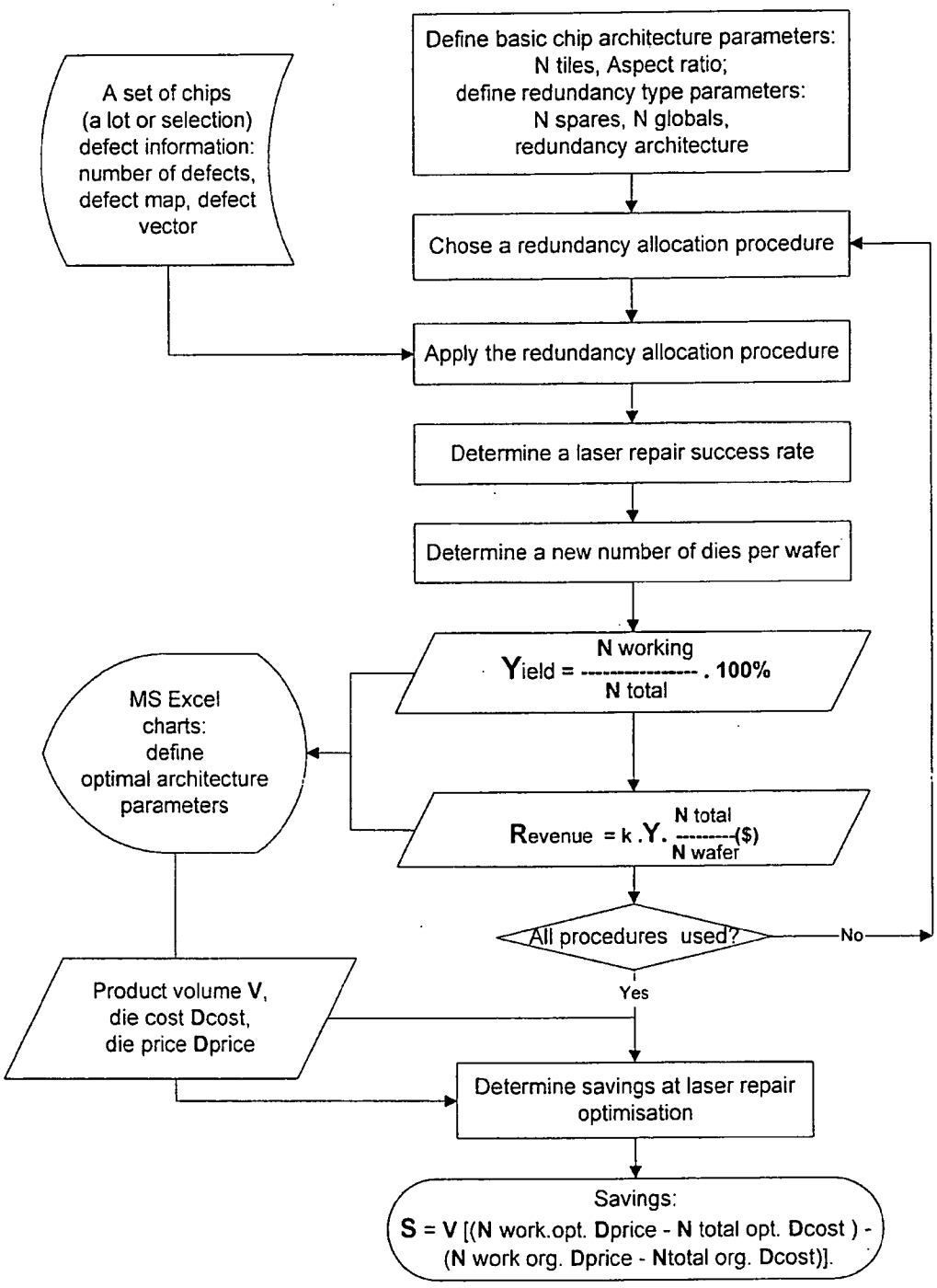
Define basic chip architecture parameters:
N tiles, Aspect ratio;
define redundancy type parameters:
N spares, N globals,
redundancy architecture
A set of chips
(a lot or selection)
defect information:
number of defects,
defect map, defect
vector
Chose a redundancy allocation procedure
Apply the redundancy allocation procedure
Determine a laser repair success rate
Determine a new number of dies per wafer
Yield = N working / N total . 100%
MS Excel
charts:
define
optimal architecture
parameters
Revenue = k . Y . N total / N wafer ($)
All procedures used?
No
Yes
Product volume V,
die cost Dcost,
die price Dprice
Determine savings at laser repair
optimisation
Savings:
S = V [(N work.opt. Dprice - N total opt. Dcost) -
(N work org. Dprice - Ntotal org. Dcost)].

Fig.8

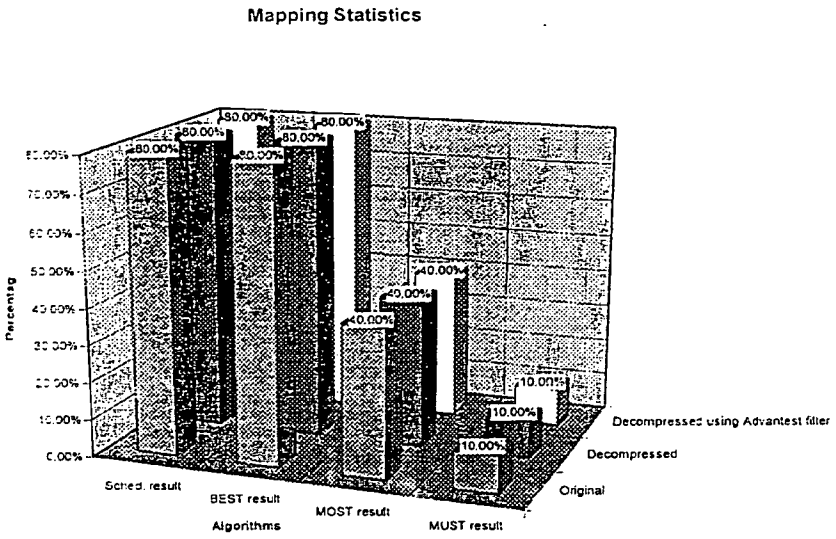
Mapping Statistics
Percentage
80.00%
40.00%
10.00%
Sched. result
BEST result
MOST result
MUST result
Algorithms
Decompressed using Advantest filter
Decompressed
Original

Fig.8a

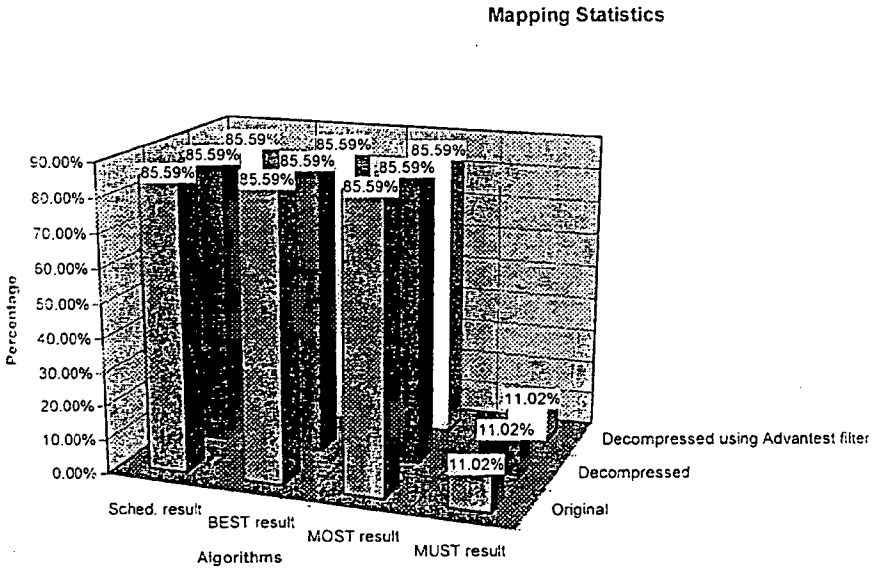
Mapping Statistics
Percentage
90.00%
80.00%
70.00%
60.00%
50.00%
40.00%
30.00%
20.00%
10.00%
0.00%
85.59%
11.02%
Sched. result
BEST result
MOST result
MUST result
Algorithms
Decompressed using Advantest filter
Decompressed
Original

Fig.8b

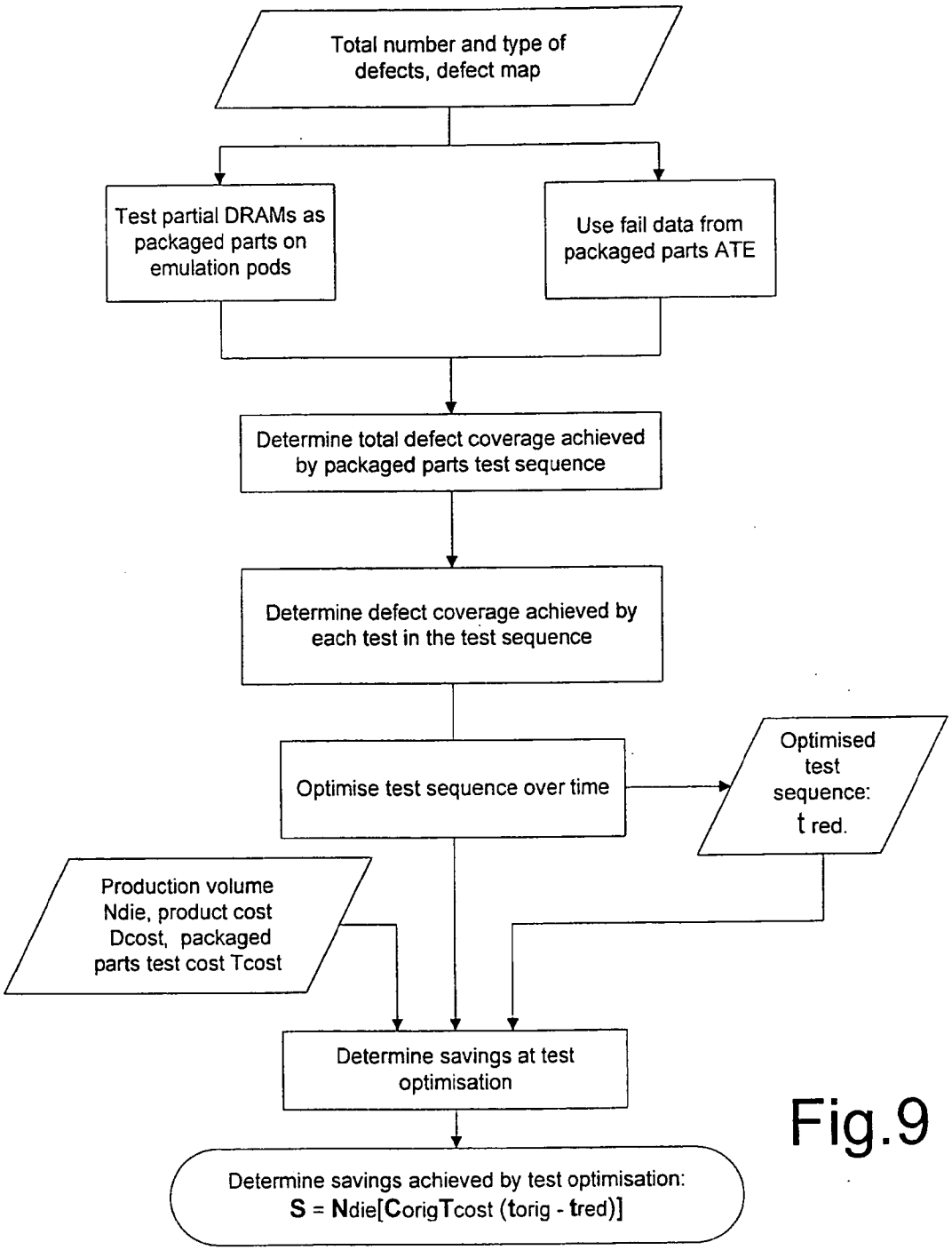
Total number and type of defects, defect map
Test partial DRAMs as packaged parts on emulation pods
Use fail data from packaged parts ATE
Determine total defect coverage achieved by packaged parts test sequence
Determine defect coverage achieved by each test in the test sequence
Optimise test sequence over time
Optimised test sequence: t red.
Production volume Ndie, product cost Dcost, packaged parts test cost Tcost
Determine savings at test optimisation
Determine savings achieved by test optimisation:
S = Ndie[CorigTcost (torig - tred)]

Fig.9

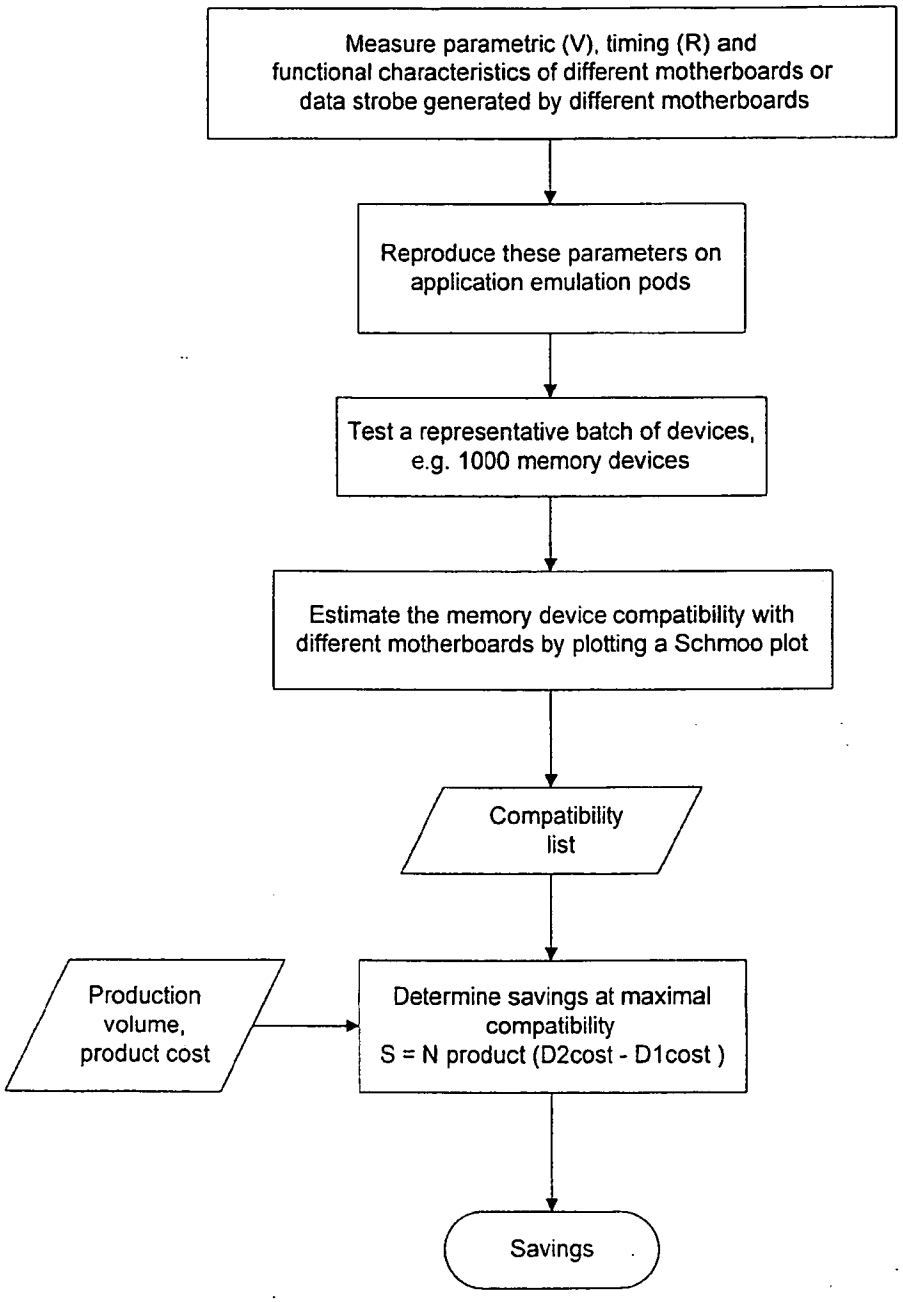
Measure parametric (V), timing (R) and functional characteristics of different motherboards or data strobe generated by different motherboards
Reproduce these parameters on application emulation pods
Test a representative batch of devices, e.g. 1000 memory devices
Estimate the memory device compatibility with different motherboards by plotting a Schmoo plot
Compatibility list
Production volume, product cost
Determine savings at maximal compatibility S = N product (D2cost - D1cost)
Savings

Fig.10

INTERNATIONAL SEARCH REPORT

Inte: ›nal Application No
PCT/RU 98/00139

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G06F17/60

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	KOREN Z ET AL: "A model for enhanced manufacturability of defect tolerant integrated circuits" PROCEEDINGS. 1991 INTERNATIONAL WORKSHOP ON DEFECT AND FAULT TOLERANCE ON VLSI SYSTEMS (CAT. NO.91TH0395-4), HIDDEN VALLEY, PA, USA, 18-20 NOV. 1991, pages 81-92, XP002092139 ISBN 0-8186-2457-4, 1991, Los Alamitos, CA, USA, IEEE Comput. Soc. Press, USA	1,3-8, 13-24
Y	see page 81, line 1 - page 84, line 32	6,9,16
	-/--	

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
3 February 1999	18/02/1999

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Pedersen, N

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Inte onal Application No
PCT/RU 98/00139

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
X	MALY W: "Computer-aided design for VLSI circuit manufacturability" PROCEEDINGS OF THE IEEE, FEB. 1990, USA, vol. 78, no. 2, pages 356-392, XP002092140 ISSN 0018-9219	1-4, 10-12, 18-23
Y	see page 380, column 1, line 22 - page 383, column 2, line 9	9
Y	STEWART D M: "Production test and repair of 256K dynamic RAMS with redundancy" INTERNATIONAL TEST CONFERENCE 1983. PROCEEDINGS, PHILADELPHIA, PA, USA, 18-20 OCT. 1983, pages 471-474, XP002092141 ISBN 0-8186-0502-2, Oct. 1983, Silver Spring, MD, USA, IEEE Comput. Soc. Press, USA	6,16
A	see page 471, column 2, line 6 - page 472, column 2, line 20 see figure 1	1-5, 7-15, 17-24
X	MOZUMDER P K ET AL: "Statistical control of VLSI fabrication processes" IEEE TRANSACTIONS ON COMPONENTS, HYBRIDS, AND MANUFACTURING TECHNOLOGY, SEPT. 1991, USA, vol. 14, no. 3, pages 467-475, XP002092142 ISSN 0148-6411 see page 174, column 1, line 1 - page 175, column 1, line 25 see page 178, column 2, line 23 - page 179, column 1, line 13	1,3-8, 18-24
A	US 5 663 891 A (BAMJI CYRUS ET AL) 2 September 1997 cited in the application see column 2, line 1 - column 2, line 30 see figure 1	1-24
A	US 4 922 432 A (KOBAYASHI HIDEAKI ET AL) 1 May 1990 cited in the application see column 2, line 5 - line 49	1-24

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

Inte[illegible]onal Application No
PCT/RU 98/00139

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5663891 A	02-09-1997	NONE	
US 4922432 A	01-05-1990	DE 3900750 A	27-07-1989
		GB 2213967 A,B	23-08-1989
		JP 1309185 A	13-12-1989
		NL 8900084 A,B,	01-08-1989
		US 5197016 A	23-03-1993